CALIBRATION AND SERVICING HANDBOOK

for

THE DATRON 4200

AUTOCAL AC STANDARD

Volume 1

Calibration and Servicing Information

850056

Issue 1 (May 1986)

For any assistance contact your nearest Datron Sales and Service Centre.
Addresses can be found at the back of this handbook.

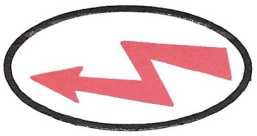
Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your instrument serial number are available on request.

X 60134O
93/03924

DANGER
HIGH VOLTAGE

THIS INSTRUMENT IS CAPABLE OF DELIVERING

A LETHAL ELECTRIC SHOCK!



FRONT or REAR terminals carry the Full Output Voltage.

THIS CAN KILL!

Guard terminal is sensitive to over-voltage

It can damage your instrument!

Unless **you** are **sure** that it is **safe** to do so,
DO NOT TOUCH the
I+ I− Hi or **Lo leads** and **terminals**

DANGER

CONTENTS

ILLUSTRATIONS

SECTION 1

CALIBRATION

1.1 INTRODUCTION

1.1.1 Manufacturer's Initial Calibration

The 4200 is fully calibrated before leaving the factory, and remains within the appropriate specification for the time periods detailed in Section 6 of the User's Handbook.

Caution

Removal of the Top Ground/Guard Assembly invalidates the manufacturer's calibration certification.

1.1.2 Need to Recalibrate

Sections 1.2 to 1.5 detail the procedures necessary to recalibrate instrument functions to known specifications. The occasions for recalibration are as follows:

1. PERIODIC ROUTINE AUTOCALIBRATION

The specifications for the 4200 are based on standard intervals of up to 24 hours, 90 days or 1 year from calibration. Users may wish to choose alternative schemes, accounting for:

a. The accuracy required when in use,

b. The scheduled calibration intervals normally adopted by the user's organization, and

c. The instrument specifications (User's Handbook Section 6)

2. RE-STANDARDIZATION

Occasions may arise when it is necessary to trim the instrument's internal Master Reference.

For example, when the 4200 is to be made traceable to a different National Standard, after transportation from one country to another.

The procedure for "STD" autocalibration is detailed in Section 1.2.8.
(Refer to Section 1.2.8, para 3, note C).

3. SPOT FREQUENCIES

The 4200 stores the spot frequencies, and their amplitude corrections, in memories which are separate from those used for wideband corrections.

Enhanced accuracy is obtained as any flatness errors in the wideband correction are eliminated. Accuracy tables are given in Section 6 of the User's Handbook, with an example showing Spot F linearity.

4. BATTERY CHANGE

The Lithium battery which powers the non-volatile calibration memory should be replaced after 5 years (Refer to Section 5.3).

After replacement, a full Pre-calibration is required (Section 1.4) followed by a Routine Autocalibration (Section 1.2).

5. CRITICAL PARTS

Recalibration (or Verification) is necessary after replacement of a critical PCB assembly or a critical component.

These are listed in Table 1.1, indicating the extent of the recalibration necessary.

1.1.3 Recalibration Procedures in this Section

(See Section 7 of the User's Handbook for Verification Procedures).

Routine Autocalibration
(Section 1.2)

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when Pre-cal is called for (Refer to Table 1.1).

Remote Calibration over the IEEE 488 Bus
(Section 1.3)

Section 1.3 describes the device-dependent commands necessary for routine calibration of the 4200 over the IEEE 488 bus, as a supplement to Section 5 of the User's Handbook. A guideline example is given, but this needs to be adapted for the bus controller in use.

Pre-calibration Procedures
(Section 1.4)

In an initial internal calibration process at manufacture, certain "Pre-cal" parameters are established in a special calibration memory.

Under certain conditions (detailed in Table 1.1) these parameters need to be re-established by the 'Pre-Cal' procedure in Section 1.4, before the Routine Autocalibration of Section 1.2.

Current Option Internal Adjustment
(Section 1.5)

If the Power Supply/Current Heatsink has been changed it may be necessary to adjust the quiescent bias current (I_Q) by internal adjustment. Refer to Section 5.4 for further information.

Assembly	Components Replaced	Precal required	Routine recal
Digital (7.2)	Complete Assembly	Full	Full
	Lithium Battery (Sect. 5.3)	Full	Full
	Non-volatile RAM (M10/M23)	Full	Full
	Non-volatile RAM Supply-Commutator components	Full	Full
Reference Divider (7.4)	Complete Assembly	Full	Full
	Reference Assembly (7.4-7)	Full	Full
	Any set of main, guard or LSD switch FET's	Full	Full
	Reference Buffer	Full	Full
	Switch Driver Flip Flops or their preselected resistors	Full	Full
	R79	Full	Full
Output Control (7.5)	Complete Assembly	—	Full
Sine Source (7.6)	Complete Assembly	Specification Verification at user's discretion	
AC (7.7)	Complete Assembly	—	Full
	Sense Amplifier	—	Full
	Reference Inverter	—	Full
	AC/DC Transfer & Integrators	—	Full
Current (7.8)	Complete Assembly	—	All I Ranges
	M8 and associated components	—	All I Ranges
	Current Shunts		All I Ranges
	Feedback resistor R45		All I Ranges
All Other Assemblies Not Specified Above		Specification Verification at user's discretion	

TABLE 1.1 LIST OF CRITICAL PCBS AND COMPONENTS

1.2.1 Introduction

The 4200 possesses excellent short and long term stability. Some users will wish to maintain the highest accuracy by recalibrating at short intervals (e.g. every 24 hours). In these cases, recalibration of the 4200 becomes a routine task. For this reason, Routine Autocalibration procedures are repeated in Section 8 of the User's Handbook. It is emphasized that the 4200 can be used immediately after recalibration.

1.2.2 The 4200 Autocal Feature

Full or part calibration may be carried out for all routine purposes from the front panel. Removal of covers is unnecessary, therefore avoiding thermal disturbance. Calibration corrections are stored in an internal memory which remains energized by a battery even when the instrument power supply is switched off. The life of the battery is estimated at 10 years, and it is normally changed at 5 year intervals. On power-up, the 4200 performs a self-test which includes a check of the contents of the calibration memory.

1.2.3 Equipment Requirements

This summary relates to the recommended method of calibrating the 4200:

AC VOLTAGE
(IV - 1000V Full Range Values and 10V Range Linearity)

An Adjustable DC Voltage Source of suitable accuracy.
Example:
Datron 4000 or 4000A Autocal Standard.

An AC/DC Thermal Transfer Standard capable of operating over the range 1V to 1100V RMS.

AC VOLTAGE
2-WIRE COMPENSATION AT HIGH FREQUENCY
(1V and 10V Full Range values)

An AC voltmeter of suitable accuracy.
Example: Datron 1081

AC MILLIVOLTS
(1mV - 100mV Full Range Values)

At LF and HF;
An AC DVM of suitable accuracy and frequency response.
Example: Datron 1081 or similar.

at LF;
A commercially-available Inductive Voltage Divider of suitable accuracy and frequency response; with ratios of 10:1, 100:1 and 1000:1.

at HF;
The 4200 under test with the correction figure for 10% of its 10V Range at HF.

AC CURRENT
(1mA - 1A Full Range Values)

A DC Current Source of suitable accuracy, and an AC/DC Thermal Transfer complete with a set of Calibrated Thermal-Transfer Current Shunts of suitable accuracy.

AC CURRENT (Alternative Method)
(1uA - 1A Full Range Values)

A set of calibrated AC Shunts of suitable value and accuracy, and

An AC DVM of suitable accuracy and frequency response.
Example: Datron 1081 or similar.

1.2.3.1 Notes on the Use of the Thermal Transfer

Four points are important:

1. **Start with OUTPUT OFF.**
The 4200 should be connected to the Thermal Transfer Standard only when the 4200 OUTPUT OFF LED is lit. (With Output OFF, the I+, I−, Hi and Lo terminals are at high impedance).

2. **Sensitivity.**
Always set the Thermal Transfer Standard to its lowest sensitivity before connecting up. Increase sensitivity when necessary to obtain the required input level.

3. **WARNING**
During Performance checks and calibration the full range voltage is present at the Thermal Transfer Standard input terminals. On 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the Thermal Transfer Standard sensitivity.

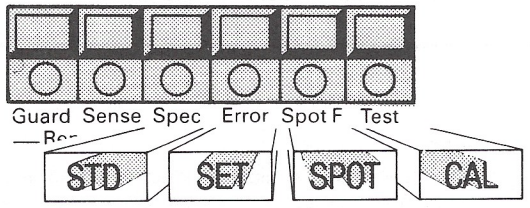
4. **CAUTION**
The Thermal Transfer Standard used must be able to withstand peak voltages up to 1600V between its input terminals. Such voltages may be present during the time that the 4200 is ramping from zero to 1100V Full Scale after setting OUTPUT ON.

1.2.4 Interconnections

Interconnection instructions in this section are necessarily simple and basic. It is recognised that they may need to be adapted to meet an individual user's requirements. It is assumed that users will possess knowledge of the operation and use of standards equipment.

1.2.5 Calibration Modes

Special keys are used in the Autocal mode. They are illustrated below:



The three keys labelled **STD, SET** and **SPOT** preselect alternative calibration modes. To finally implement any calibration, the **CAL** key must be pressed.

Fig. 1.1 CALIBRATION MODES

These keys are activated by a simple procedure:

On the rear panel there are two switches: the IEEE 488 address switch, and a security keyswitch labelled 'RUN/CAL ENABLE'.

By setting the address switch to 31 (ADD 11111) for Front Panel calibration, and the keyswitch to CAL ENABLE; four of the front panel 'MODE' keys are reassigned to calibration functions, permitting access to the correction memories.

When these modes are active, the legend 'cal' is presented on the MODE display.

1.2.5.1 General Procedure

The OUTPUT display is set to the Calibration Standard value, the 4200 output is switched ON, and one of the calibration mode preselector keys (STD, SET or SPOT) is pressed. The 4200 output is adjusted to equal the Calibration Standard value, and the CAL key is pressed to execute the calibration.

1.2.5.2 Autocal Facilities

SET — The SET key allows calibration to any value between 20% and 200% of nominal Full Range value (20% to 110% on 1000V range). If, for instance, an adjustable DC voltage standard is not available, the SET key permits the 4200 to be calibrated against a Thermal Transfer standard whose reference is a buffered bank of Standard Cells.

SPOT — When SPOT is pressed, the 4200 assumes that the spot frequency is to be changed, and so defaults frequency to 1kHz. When used with SET, SPOT calibration can be carried out within 10% of full range value, but when SPOT is used without SET, the 4200 assumes that the calibration is to be at Full Range. After SPOT calibration, selecting Spot F at the calibrated value achieves the highest possible specification. For Recall procedures see the User's Handbook Section 4, page 4-11.

STD — The STD key allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long term drift, or to avoid a full recalibration of the 4200 when Laboratory References have been re-standardized. STD calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available on either the 1V or 10V range.

CAL — The CAL key executes, then cancels, the preselected AUTOCAL mode.

CAL only — If the CAL key is pressed without first pressing SET, SPOT or STD, the 4200 assumes that the selected range is to be calibrated at the exact Full Range, at either LF or HF or both.

1.2.6 General Notes

Remote Sense is available as follows:

1V 10V 100V 1000V	- Local/Remote Sense
1mV 10mV 100mV	- Local Sense only
All current ranges	- not applicable

(Local = 2-wire sense; Remote = 4-wire sense)

Output must be OFF to change sense connection (except that Remote changes automatically to Local when switching to Millivolt Ranges).

On 1V and 10V ranges a Local/Remote difference correction can be stored; for the calibration procedure refer to Section 1.2.9.

Upranging — OUTPUT OFF Default.
The 4200 cannot enter High-Voltage State (>75V) with OUTPUT ON. Consequently, when ranging-up, the operating system allows the upranging to occur, but defaults to OUTPUT OFF for two specific cases:

a. When upranging to the 1000V Range,
b. When upranging to the 100V Range; to a voltage of 75V or more.

Otherwise, OUTPUT remains ON when changing OUTPUT RANGE (refer to User's Handbook Section 4, pages 4-7 and 4-8).

High Frequency Calibrations. Several iterations may be required to achieve satisfactory calibration; particularly if the initial errors are large, or if the Transfer System being used imposes a long calibration time.
Repeat the procedure as necessary.

1000V Range Calibration Sequence: LF calibration must be completed first. However HF1/HF2 bands may, if the user requires, be calibrated in reverse order.SET mode must be used for 700V/HF2.

SPOT Memory Erasure. To prevent unwanted calibrations at unused spot frequencies, it is possible to 'Uncalibrate' any spot frequency on any range. The procedure is:

Select **Zero** Output, set **OUTPUT ON** and Press **CAL.** When the CAL-ENABLE/RUN Switch is set to RUN, any subsequent selection of that particular Spot F will cause the message 'SFX---' to appear on the MODE/FREQUENCY display (X is the store number). This indicates that the spot is uncalibrated.

1.2.7 Calibration Sequence

The sequence of operations for full calibration of the 4200 Autocal Standard is given below:

Preparation	Section 1.2.7.1
AC Voltage	1.2.8
2-wire HF compensation	1.2.9
AC Current	1.2.10
Return to use	1.2.7.2

WARNING: During performance checks and calibration a common mode voltage equal to the full range voltage may be present at the Thermal Transfer input terminals. On 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the Thermal Transfer sensitivity.

CAUTION: The Thermal Transfer Standard used must be able to withstand peak voltages up to 1600V between its input terminals. Such voltages may be present during the time that the 4200 is ramping from zero to 1100V Full Scale after setting OUTPUT ON.

1.2.7.1 Preparation

Before any calibration from the front panel is carried out, prepare the 4200 as follows:

1. Turn on the instrument to be checked and allow minimum of 4 hours to warm-up in the specified environment.
2. IEEE 488 Address switch:
   Set to ADD 11111 as shown (Address 31).
3. CALIBRATION ENABLE Key switch (Rear Panel).
   Insert Calibration Key and turn to ENABLE.

These actions activate the four calibration modes (labelled in red), and present the 'cal' legend on the MODE display.

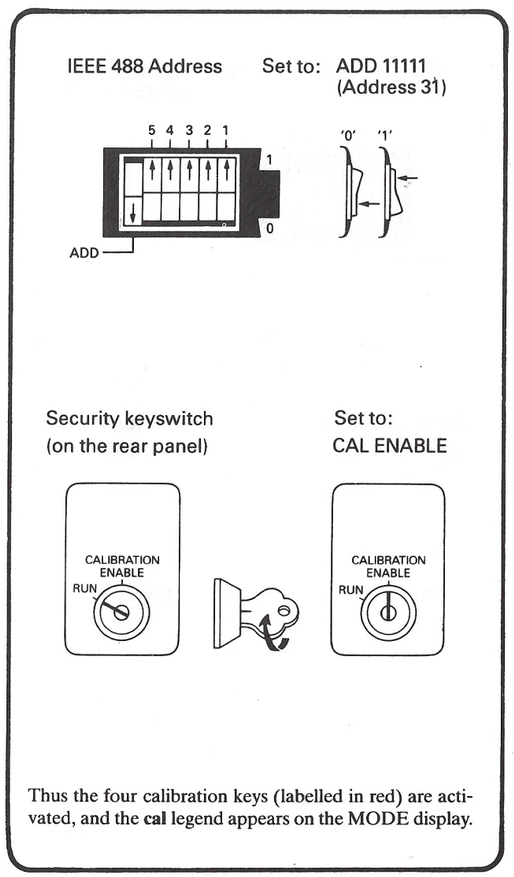
4. Ensure that the OUTPUT OFF LED is lit.

1.2.7.2 Return to Use

When any calibration is completed, return the 4200 to use as follows:

1. Ensure that the OUTPUT OFF LED is lit.
2. CALIBRATION ENABLE key switch (Rear Panel):
   Turn to RUN and remove the calibration key.
3. IEEE 488 Address switch:
   Restore to the correct address if the 4200 is to be used in an IEEE 488 system.

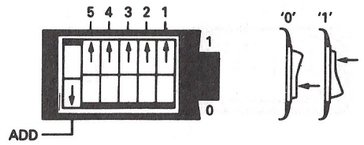
The activation procedure is illustrated below:



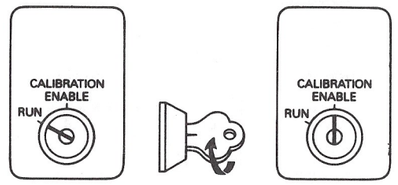
Thus the four calibration keys (labelled in red) are activated, and the **cal** legend appears on the MODE display.

The activation procedure is illustrated below:

IEEE 488 Address **Set to: ADD 11111 (Address 31)**

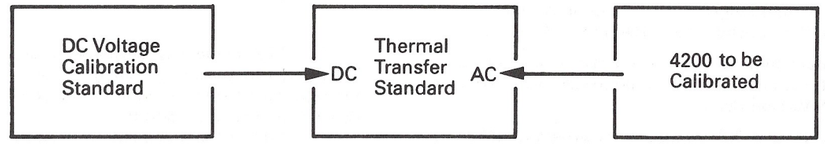


Security keyswitch (on the rear panel) **Set to: CAL ENABLE**



Thus the four calibration keys (labelled in red) are activated, and the cal legend appears on the MODE display.

1.2.8 AC Voltage Full Range Calibration (1V–1000V)
(Using Thermal Transfer Standard and DC Calibration Standard)



Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required as part of the following procedure:

WARNING:

THE TERMINALS MARKED WITH THE SYMBOL CARRY THE OUTPUT OF THE 4200. THESE TERMINALS AND ANY OTHER CONNECTIONS TO THE LOAD UNDER TEST COULD CARRY LETHAL VOLTAGES. UNDER NO CIRCUMSTANCES SHOULD USERS TOUCH ANY OF THE FRONT (OR REAR) PANEL TERMINALS UNLESS THEY ARE FIRST SATISFIED THAT NO DANGEROUS VOLTAGE IS PRESENT.

Note

Any existing stored HF 2-wire compensation is cleared during normal 4-wire HF calibration. The procedure in Section 1.2.9 allows a user to re-establish HF compensation for 2-wire measurement.

Nominal Cal. Points for 1V to 1000V Ranges.

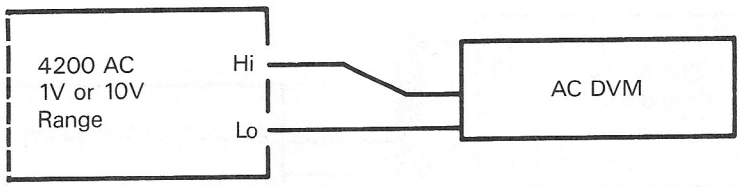
DC Standard OUTPUT Voltage	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
1.000000V	1V 1kHz	1.000000V	LF
1.000000V	1V 1MHz	1.000000V	HF
10.00000V	10V 1kHz	10.00000V	LF
10.00000V	10V 1MHz	10.00000V	HF
100.0000V	100V 1kHz	100.0000V	LF
100.0000V	100V 100kHz	100.0000V	HF
1000.000V	1000V 1kHz	1000.000V	LF
1000.000V	1000V 30kHz	1000.000V	HF1

700V at 100kHz:
'SET' Calibration must be employed.

700.000V	1000V 100kHz	700.000V	HF2

1. **4200 & DC Voltage Standard**
With OUTPUT OFF, connect to the Thermal Transfer AC and DC inputs, respectively.
2. **Thermal Transfer Standard**
Configure for DC measurement at the required Calibration Voltage.
3. **DC Voltage Calibration Standard**
Set to the Cal. voltage, OUTPUT ON.
4. **Thermal Transfer Standard**
   a. Adjust for Null at the Cal. Voltage.
   b. Configure for AC measurement at the Cal. Voltage.
5. **4200**
   a. On AC FUNCTION, select the required OUTPUT RANGE.
   b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).
   c. Use FREQUENCY ↑↓ keys to display the required Cal. Frequency.
   d. Use OUTPUT ↑↓ keys to display the required Cal. Voltage (if at Nominal Full Range, merely press the Full Range key).
   e. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   f. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer.
   g. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect).

1.2.9 AC Voltage - HF 2-wire Compensation (1V & 10V range).
(Using an AC DVM)



Calibration of HF 2-wire Compensation

On the 1V and 10V ranges there are two HF calibration memories. One holds the correction value obtained during Remote Sense (4-wire) 'wideband' calibration; the other contains a 2-wire HF compensation value which is added to the wideband correction, when Remote Sense is not selected (local sense).

During a 4-wire HF calibration on the 1V or 10V range, the stored HF 2-wire compensation value is cleared to zero. Any 4-wire HF calibration to be performed must therefore be completed before the 2-wire compensation is executed.

Calibrate the 4200 at or close to the calibration points in the table, selecting SET as required.

Nominal Cal. Points for 2-wire HF Compensation.

DC Standard OUTPUT Voltage	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
1.000000V	1V 1MHz	1.000000V	HF
10.00000V	10V 1MHz	10.00000V	HF

1. **4200 & AC Voltmeter**
With 4200 OUTPUT OFF, make 4-wire connections between the 4200 and the AC DVM.

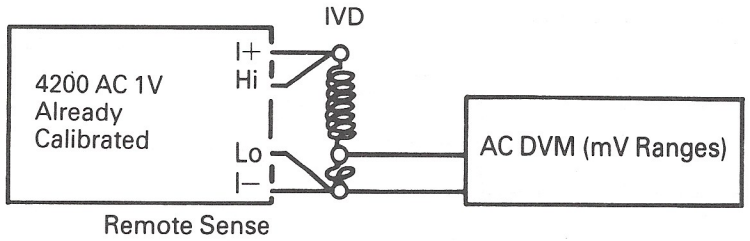
2. **AC Voltmeter**
Configure for AC measurement at the required Calibration Voltage.

3. **4200**
   a. On AC FUNCTION, select the required OUTPUT RANGE.
   b. Select the required FREQUENCY RANGE.
   c. Use the FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   d. Use the OUTPUT ↑↓ keys to display the required Calibration Voltage.
   (If at Nominal Full Range, merely press the Full Range key.)

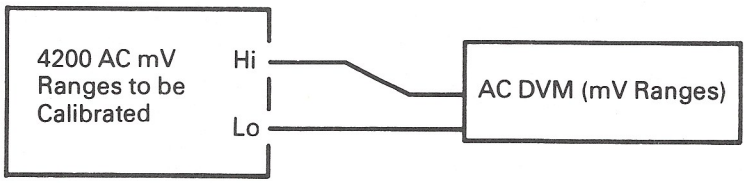
4. **HF 2-wire Calibration Sequence**
   a. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   b. Record the DVM reading.
   c. Set 4200 OUTPUT OFF.
   d. On the 4200 deselect Remote Sense.
   e. Connect the DVM to the 4200 Hi and Lo terminals for 4-wire measurement of the 4200 2-wire output.
   f. Set 4200 OUTPUT ON.
   g. Use the 4200 OUTPUT ↑↓ keys to display the DVM reading recorded at (b).
   h. Press 'CAL'

1.2.10 Millivolts (LF) Full Range Calibration (1mV–100mV)

(Using calibrated 4200 1V Range, Inductive Voltage Divider (IVD) and AC DVM)



Standardization of DVM Millivolt Ranges



Calibration of 4200 LF Millivolt Ranges

Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:

It is assumed that for a SPOT calibration, the 1V Range has already been Spot calibrated at the required calibration point.

Nominal Cal. Points for Millivolt Ranges.

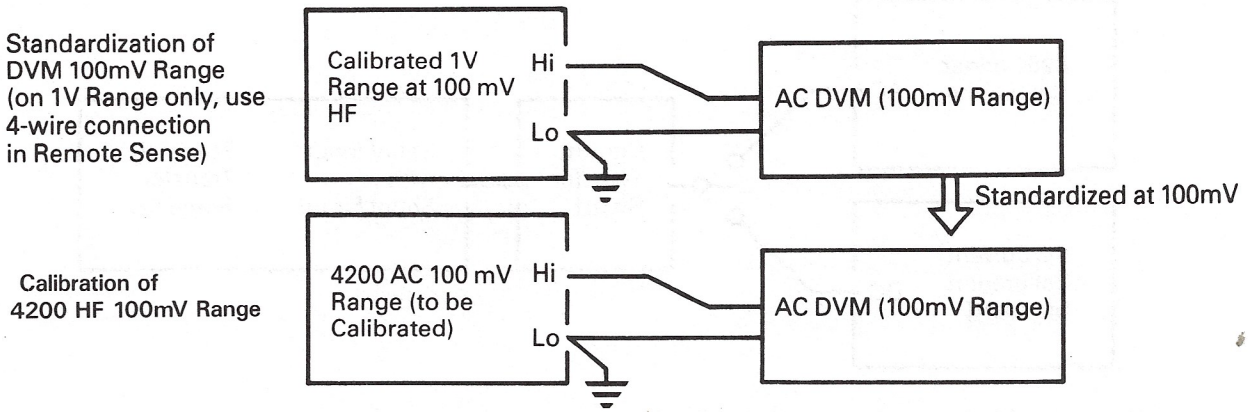
IVD Ratio (1V Range to mV Range)	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
10 : 1	100mV 1kHz	100.0000mV	LF
100 : 1	10mV 1kHz	10.0000mV	LF
1000 : 1	1mV 1kHz	1.0000mV	LF

1. **4200, IVD and AC DVM**
With OUTPUT OFF, connect the circuit for Standardization.

2. **IVD**
Set the ratio as required for the Millivolt Range to be calibrated.

3. **AC DVM**
Configure for measurement at the required Calibration Point.

4. **4200**
   a. On AC FUNCTION, select 1V RANGE.
   b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).
   c. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   d. Use OUTPUT ↑↓ keys to display the required IVD input voltage.
   (If at Nominal Full Range, merely press the Full Range key.)
   e. Set OUTPUT ON; note DVM reading as 'V1'.
   f. Set OUTPUT OFF, and reconnect the circuit for Calibration.
   g. Select the required Millivolt OUTPUT RANGE.
   h. Use OUTPUT ↑↓ keys to set the Calibration Voltage on the OUTPUT Display.
   (If at Nominal Full Range, merely press the Full Range key.)
   j. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   k. Use the ↑↓ keys to adjust the OUPUT Display reading to obtain 'V1' on the DVM.
   l. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.



N.B.

These Calibrations are not fully traceable. Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:

It is assumed that the 1V and 10V Ranges have been Wideband-calibrated (and for SPOT calibration, the 1V Range has already been Spot calibrated) at the required HF calibration points.

Nominal Cal. Points for HF Millivolt Ranges.

4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Voltage	Freq. Band set by 4200
100mV 1MHz	100.0000mV	HF
10mV 1MHz	10.0000mV	HF
1mV 1MHz	1.0000mV	HF

1. 4200 and AC DVM

a. Measure 10.00000V output on the 10V Range at the HF Calibration Frequency using the Thermal Transfer.
Note the reading: call it 'V1'.

b. Measure 1.00000V output on the 10V Range at the HF Calibration Frequency using the Thermal Transfer.
Note the reading: call it 'V2'.

c. Divide V1 by V2; divide the result by 10. This gives the 10% Range Correction Factor, 'C'.

$$C = \frac{V1}{10 \times V2}$$

This factor subsequently corrects a DVM measurement at 10% of one range, to standardize the DVM for calibration of the next millivolt range down.

d. With OUTPUT OFF, connect the circuit for Standardization.

2. 4200

a. On AC FUNCTION, select 1V OUTPUT RANGE.

b. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).

c. Use FREQUENCY ↑|↓ keys to display the required Calibration Frequency.

d. Using the OUTPUT ↑|↓ keys, adjust the OUTPUT Display to the 100mV Calibration Voltage on the 1V Range.

e. Set the 4200 OUTPUT ON and note the DVM reading. Multiply the reading by 'C', and note the results as 'Vc'.
(If the DVM being used is a Datron Autocal instrument, the Maths function can do this automatically.)

f. With OUTPUT OFF, connect the circuit for Calibration.

g. Set 4200 OUTPUT OFF, select 100mV Range, and again use the OUTPUT ↑|↓ keys to set the OUTPUT Display to the Calibration Voltage.
(If at Nominal Full Range, merely press the Full Range key).

h. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).

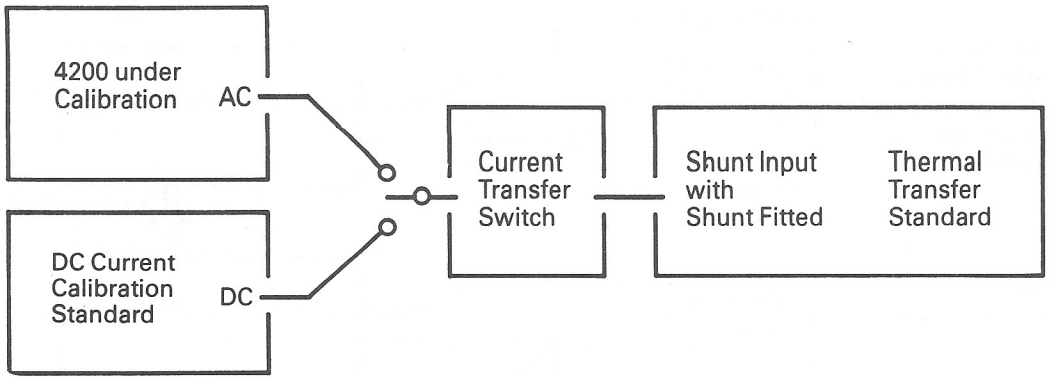
j. Adjust the OUTPUT ↑|↓ keys for a reading of 'Vc' on the DVM.

k. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, re-press the SPOT key to deselect). Set OUTPUT OFF.

l. Repeat operations 2 (a) to (k), selecting 10mV on the 100mV Range to standardize the DVM, and calibrating the 10mV Range, using the same correction factor 'C'.

m. Repeat operations 2 (a) to (k), selecting 1mV on the 10mV Range to standardize the DVM, and calibrating the 1mV Range, using the same correction factor 'C'.

1.2.12 Current Full Range Calibration (1mA–1A)
(Using Thermal Transfer, Current Shunts and DC Current Standard)



Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Calibrate 1mA Range only if the Thermal Transfer is adequately calibrated at these levels.

Nominal Cal. Points for 1mA to 1A Ranges.

DC Standard OUTPUT Current	4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Current	Freq. Band set by 4200
1.000000mA	1mA 300Hz	1.000000mA	LF
1.000000mA	1mA 5kHz	1.000000mA	HF
10.00000mA	10mA 300Hz	10.00000mA	LF
10.00000mA	10mA 5kHz	10.00000mA	HF
100.0000mA	100mA 300Hz	100.0000mA	LF
100.0000mA	100mA 5kHz	100.0000mA	HF
1.000000A	1A 300Hz	1.000000A	LF
1.000000A	1A 5kHz	1.000000A	HF

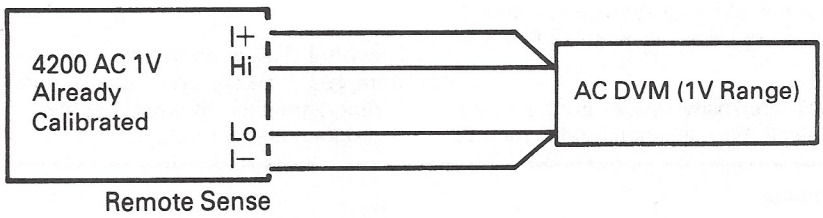
1. **Thermal Transfer Standard**
Configure for DC measurement at the required Calibration Current and connect the appropriate shunt.

2. **DC Current Standard**
   a. With OUTPUT OFF, connect across the Thermal Transfer shunt, and set to the required Calibration Current.
   b. Set OUTPUT ON.

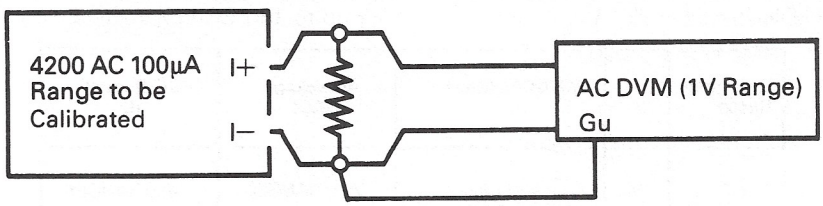
3. **Thermal Transfer Standard**
Adjust for null at the Calibration Current.

4. **DC Current Standard**
   a. Set OUTPUT OFF.
   b. Disconnect from the shunt.

5. **4200**
   a. With OUTPUT OFF, connect the I+ and I– terminals across the Shunt.
   b. On I FUNCTION, select the required OUTPUT RANGE.
   c. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 – F5).
   d. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.
   e. Use OUTPUT ↑↓ keys to display the required Calibration Current.
   (If at Nominal Full Range, press the Full Range key.)
   f. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).
   g. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a null on the Thermal Transfer.
   h. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.



Standardization of DVM 1V Range



Calibration of 4200 Current Ranges

Calibrate the 4200 at or close to the calibration points in the table, selecting SET and/or SPOT as required, as part of the following procedure:

Note:
It is assumed that for a SPOT calibration, the 1V Range has already been Spot calibrated at the required calibration point.

Nominal Cal. Points for 100μA to 1A Ranges.

4200 OUTPUT RANGE/ FREQUENCY	4200 Nominal OUTPUT Current	Freq. Band set by 4200
100μA 300Hz	100.0000μA	LF
100μA 5kHz	100.0000μA	HF
1mA 300Hz	1.000000mA	LF
1mA 5kHz	1.000000mA	HF
10mA 300Hz	10.00000mA	LF
10mA 5kHz	10.00000mA	HF
100mA 300Hz	100.0000mA	LF
100mA 5kHz	100.0000mA	HF
1A 300Hz	1.000000A	LF
1A 5kHz	1.000000A	HF

1. **4200 and AC DVM**
With OUTPUT OFF, connect the 4200 and DVM for Standardization.
Select the 1V Range on the AC DVM.

2. **4200**

a. Set to the 1V Range at the Calibration Frequency and adjust for calibrated 1.000000V output.

b. Set OUTPUT ON and note the DVM reading as 'V1'.

c. Set OUTPUT OFF, and reconnect the test circuit for Calibration, using the correct shunt for the range to be calibrated.

d. On I FUNCTION, select the required OUTPUT RANGE.

e. Select the required FREQUENCY RANGE (or if a Spot Frequency is to be calibrated: Press SPOT and select F1 - F5).

f. Use FREQUENCY ↑↓ keys to display the required Calibration Frequency.

g. Use OUTPUT ↑↓ keys to display the required Calibration Current.
(If at Nominal Full Range, press the Full Range key).

h. Set 4200 OUTPUT ON (and if NOT at Nominal Full Range, Select SET).

j. Use the OUTPUT ↑↓ keys to adjust the OUTPUT Display reading to obtain a DVM reading of 'V1'.

k. Execute the calibration by pressing the CAL key (and if calibrating a Spot Frequency, repress the SPOT key to deselect). Set OUTPUT OFF.

1.3 REMOTE CALIBRATION GUIDELINES

1.3.1 Introduction

The operation of the 4200 in systems applications, via the IEEE 488 interface, is described in Section 5 of the User's Handbook.

In addition to its capability as a programming calibrator, the 4200 can itself be calibrated under remote control. Full autocalibration of the instrument over the bus implies availability of programmable standards, a programmable thermal transfer standard and a suitably-programmed controller.

1.3.2 Calibration Commands

Table 1.2 lists the device-dependent calibration commands used in the 4200. The transfer of calibration facilities to remote control is illustrated in Fig. 1.2.

Note.

With the Calibration keyswitch set to ENABLE, the 'I' code (User's Aide-Memoire) accesses an alpha-numeric store for up to 16 ASCII characters.

Command Codes		AUTOCAL Mode	AC Voltage (AC)	AC Current (I)
CØ	CAL only	Gain calibration (at nominal FR)	ALL RANGES	ALL RANGES
C1 and CØ	SET and CAL	Gain for range at User's selected value	ALL RANGES	ALL RANGES
C2 and CØ	STD and GAIN CAL		1V and 10V Ranges only	–
C3 and CØ	PRECAL and GAIN CAL		10V Range	–
T1 to T5 and CØ	Spot Frequency 1 to Spot Frequency 5 and GAIN CAL		ALL RANGES	ALL RANGES
T1 to T5 and C1 and CØ	Spot Frequency 1 to Spot Frequency 5 and Gain for range at User's selected value		ALL RANGES	ALL RANGES
TØ	Cancel Spot Frequency		ALL RANGES	ALL RANGES
I	User's Message		See para. 1.3.2	

TABLE 1.2 AVAILABILITY OF COMMAND CODES

These commands can only be activated when two conditions have been fulfilled:

1. The CALIBRATION ENABLE keyswitch on the 4200 Rear Panel must be set to ENABLE.
2. The IEEE Interface command-code W1 must have been received and activated.

In addition the bus command C3 (PRECAL) can only be activated when the internal 'PRE-CAL ENABLE' switch is enabled.

When the 4200 is under remote control over the bus, the command code WØ overrides the settings of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

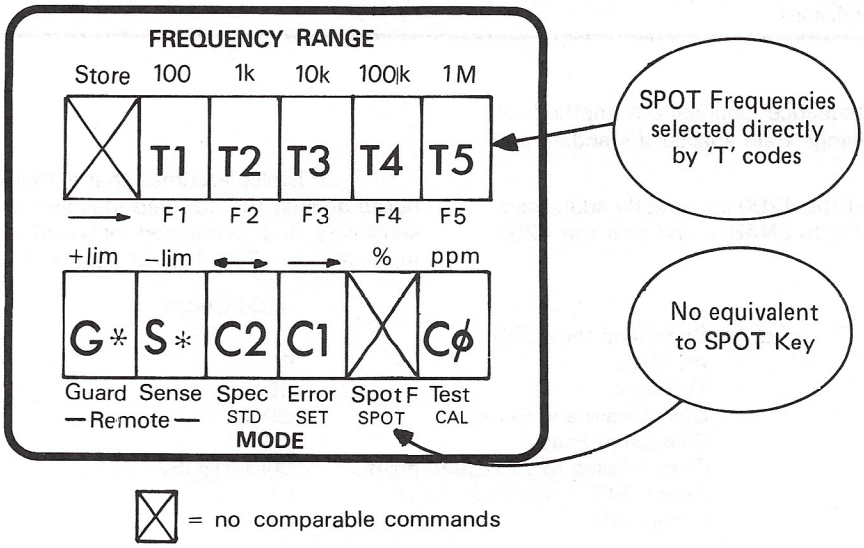


FIG. 1.2 TRANSFER OF CALIBRATION FACILITIES TO REMOTE CONTROL

1.3.2.1 General Procedure

The Main Register is set to the Calibration Standard value (M***...), the 4200 Output is switched ON (O1), and one or a specified sequence of the calibration mode command codes (C1, C2, C3, I, T1-T5) may be transmitted.

The 'M' Code is adjusted to obtain a null at the Calibration Standard value, and CØ is transmitted to execute the calibration.

1.3.2.2 Command Code Facilities

C1 (SET) C1 allows calibration to any value between 20% and 200% of nominal Full Range value (20% to 110% on 1000V range). If, for instance, an adjustable DC voltage standard is not available, C1 permits the 4200 to be calibrated against a Thermal Transfer standard whose reference is a buffered bank of Standard Cells.

C2 (STD) C2 allows a user to trim the value of the internal Master Reference voltage. The facility can be used to correct for any long-term drift, or to avoid a full recalibration of the 4200 when Laboratory References have been re-standardized.

C2 calibration effectively changes the gain of all voltage and current ranges in the same ratio, by a simple procedure available either on the 1V or 10V range.

T1-T5 (SPOT) The SPOT facility is not directly related to the manual SPOT key. The spot frequencies are directly accessible using 'T' codes, T1 to T5 corresponding to the F1 to F5 store keys, but in SPOT frequency mode. When a T code is received in calibration mode, the 4200 assumes that the spot frequency is to be changed, and so defaults frequency to 1kHz.

When a T code is used with SET; SPOT calibration can be carried out within 10% of full range value, but when used without SET, the 4200 assumes that the calibration is to be at Full Range.

After SPOT calibration, selecting Spot F at the calibrated value achieves the highest possible specification. For Recall procedures see the User's Handbook Section 4.

C3 (PRECAL) C3 is used to enable 'pre-calibration'. This is a procedure which is used at manufacture, and must also be used whenever all the calibration memories are cleared to zero (for example if the supply to the non-volatile RAM has been disrupted).

C3 accesses a special calibration memory, as part of a two-stage calibration on the 10V range. (Refer to para. 1.4.5).

CO CØ executes the programmed procedure which was previously selected by the C1; C2; T1 to T5; or C3 code. No calibration is complete until a CØ code has been received.

CAL only If CØ is sent without preselecting one of the other modes, the 4200 assumes that the selected range is to be calibrated at the exact Full Range, at either LF or HF or both.

1.3.3 Programming Guidelines

1.3.3.1 An Example

The following sequence suggests a method of calibrating the 4200 1V Range Gain against a standard cell value of +1.018057V.

It is assumed that the 4200 is correctly addressed, its Calibration Keyswitch set to ENABLE and that the 4200 Output is OFF.

It is also assumed that a Thermal Transfer has been nulled against the buffered standard cell, is now set to low sensitivity and connected between the 4200 Hi and Lo terminals as in Fig 1.1 (a) of Section 1.2.8.

		4200 Codes
a.	Command the 4200:	
	AC Volts	F1
	1V Range	R5
	Local Guard and Sense	GØ SØ
	Calibration Enable	W1
	Output Value to calibration point	M+1.018057
	Select 'SET' Calibration mode	C1
	Output ON	O1
b.	Establish null tolerance limits.	
c.	Command the Thermal Transfer: Recall Sensitivity Range and Reading; Increase Sensitivity Range and repeat recall until reading exceeds half-scale.	
d.	Calculate 4200 setting for null. Set 4200 output to calculated value.	M***...
e.	Repeat (c) and (d) until null is within limits.	
f.	Command the 4200 to execute 'CAL'	CØ.

The example suggests only the broad outline of one of many sequences which could be used to perform 4200 calibrations.

1.3.3.2 Calibration Command Strings

The following command strings are given for the sole purpose of illustrating the methodology designed into the 4200 for remote calibration modes. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the 4200 has previously been programmed in function and range (not autorange RØ) and that the external circuit is set up correctly. The 4200 is already programmed into its calibration mode by W1, with the calibration keyswitch set to ENABLE, and output OFF.

a. Nominal Full Range LF Gain Calibration:
H(LF) A1 O1=M (for null)=CØ=OØ=

b. Nominal Full Range HF Gain Calibration:
H(HF) A1 O1=M (for null)=CØ=OØ=

c. Combined Nominal LF and HF Gain Cal:
H(LF) A1 O1=M (for null)=C0=
H(HF)=M (for null)=C0=O0=

d. Non-nominal LF Gain Calibration:
H(LF) M(20%–200% FR) C1=
O1=M(for null)=CØ=OØ=

e. Non-nominal HF Gain Calibration:
H(HF) M(20%–200% FR) C1=
O1=M (for null)=C0=O0=

f. Combined Non-nominal LF and HF Gain Cal:
H(LF) M(20%–200% FR) C1=
O1=M(for null)=CØ=
H(HF) M(20%–200% FR) C1=
M(for null)=CØ=OØ=

g. SPOT Calibration at Nominal Full Range:
T(1 to 5) H(required spot frequency)
A1 O1=M(for null)=CØ=OØ=

h. SPOT Calibration at a value within ± 10% of Full Range:
T(1 to 5) H(required spot frequency)
M(± 10% FR) C1=O1=M(for null)=CØ= OØ=

j. Standardization at Nominal Full Range (1V or 10V Range only):
H(LF) A1 C2 O1=M(for null)=CØ=OØ=

k. Standardization at a Non-nominal value (1V or 10V range only):
H(LF) M(20%–200% FR) C2=
O1=M(for null)=CØ=OØ=

The string for code C3 appears in para 1.4.5.2.

1.4 PRE-CALIBRATION

For all normal purposes, the routine procedures detailed in Section 1.2 (and repeated in the User's Handbook Section 8) are sufficient to maintain 4200 calibration.

In an initial internal calibration process at manufacture, certain 'PRE-CAL' parameters are established in a special calibration memory to define the overall linearity of the 4200, and to allow maximum routine calibration memory span for adjustments. Thereafter all routine calibrations may be performed from the front panel or over the IEEE Interface without removing the covers.

The stored parameters are invalidated by replacement of certain critical parts of the instrument; detailed below.

After replacement of any of these parts, new parameters must be stored in the PRE-CAL memory, by procedures (in manual or remote control) detailed in this section.

NB. Removal of the upper or lower Guard/Ground shields invalidates any previous calibration by the Datron Factory or Service Centre.

Critical Parts

1. The Lithium battery which powers the whole calibration memory when the instrument supply is switched off. This should be replaced at five-year intervals.
   (Refer to Section 5.3).

The following parts are normally replaced only on failure. A full list appears in Section 1.1 Table 1.1.

2. The Digital Assembly
3. The Reference Divider Assembly
4. Critical components in the Digital or Reference Divider, AC and Sine Source assemblies

Pre-Calibration must be followed by a full Routine Calibration of the whole instrument (Section 1.2).

1.4.1 Validity

The adjustments detailed in the following sequences include intentionally clearing the instrument's calibration memory, which loses all previous calibration information.

Therefore before proceeding make certain that the reasons for carrying out a complete recalibration are valid. (If in any doubt, consult your Datron Service Center).

1.4.2 Calibration Standards Equipment Required

1. A precision voltmeter capable of 1V AC measurement with a stability between readings of better than ± 5ppm.
   Example: Datron Instruments 1081
2. An inductive voltage divider with ratios of x1.0 and x0.1 capable of dividing 10.000,00V to 1.000,000V to an accuracy better than ± 1ppm.

1.4.3 Preparation

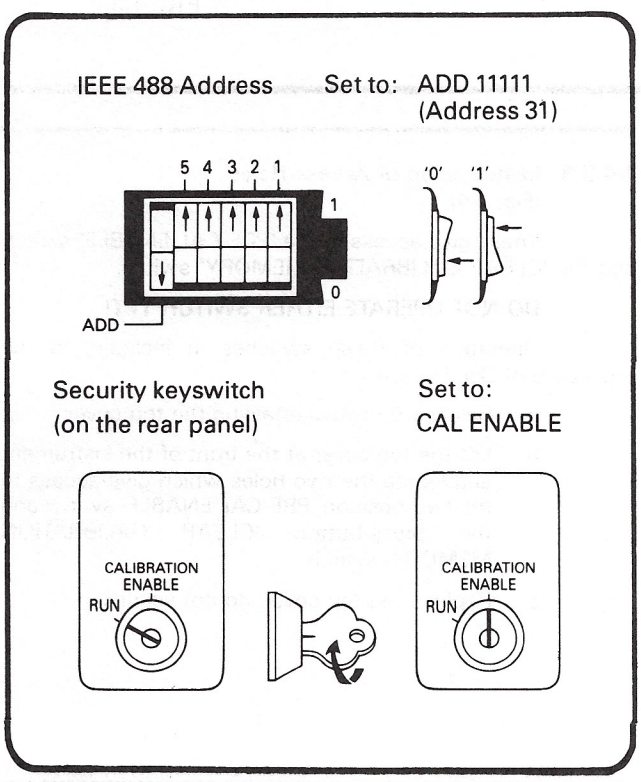
1.4.3.1 Manual Calibration Mode

Before any calibration is carried out, prepare the 4200 as follows:

a. Turn on the instrument to be checked and allow a minimum of 4 hours to warm-up in the specified environment.

b. IEEE 488 Address switch:
Set to ADD 11111 as shown (Address 31).

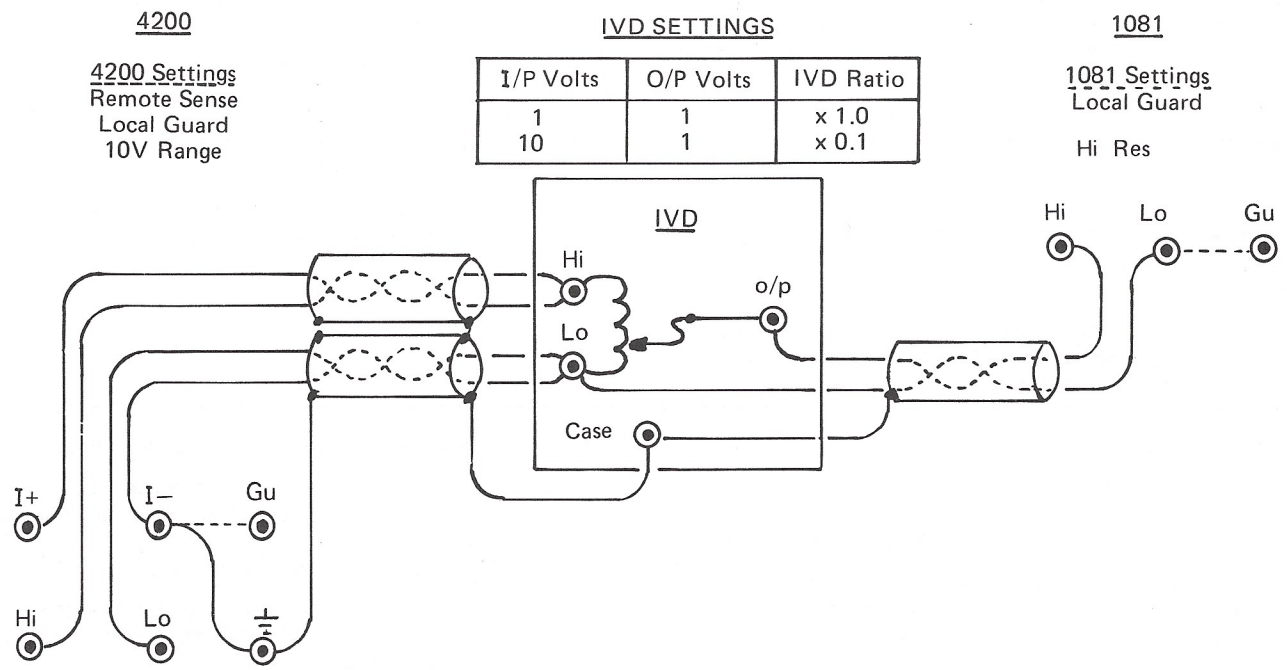
c. CALIBRATION ENABLE key switch:
Insert Calibration Key, and turn to ENABLE.



1.4.3.2 Interconnections

a. Ensure the 4200 OUTPUT OFF LED is lit.
Cancel any MODE keys.
Select Remote Sense.
Deselect Remote Guard.
Select the 1kHz Frequence Range.

b. Select ACV FUNCTION and connect the IVD to the 4200 terminals as shown. Use short leads.



I/P Volts	O/P Volts	IVD Ratio
1	1	x 1.0
10	1	x 0.1

FIG. 1.3

1.4.3.3 Identification of Access Holes
(Fig. 1.4)

These give access to the 'PRE-CAL ENABLE' switch and the 'CLEAR CALIBRATION MEMORY' switch.

DO NOT OPERATE EITHER SWITCH YET!

Operation of these switches in included in the procedure of Section 1.4.4.

a. Release 6 screws retaining the top cover.

b. Lift the top cover at the front of the instrument and locate the two holes which give access to the two-position 'PRE-CAL ENABLE' switch and the press-button 'CLEAR CALIBRATION MEMORY' switch.

c. Replace the top cover, do not secure.

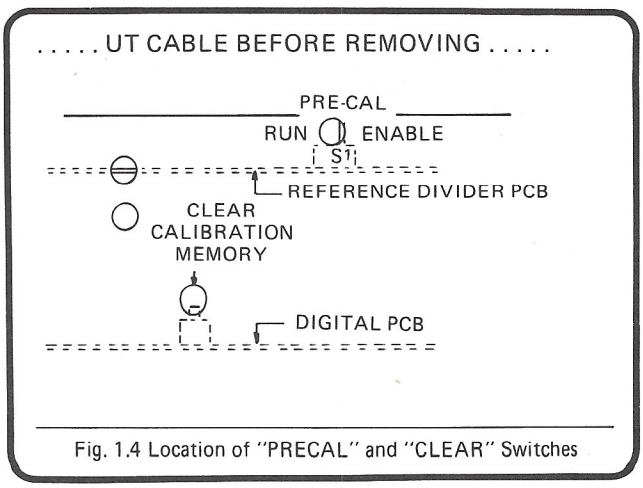


Fig. 1.4 Location of "PRECAL" and "CLEAR" Switches

1.4.4.1 'PRE-CAL ENABLE' and 'CALIBRATION MEMORY CLEAR' Switches

a. Cover
Lift the top cover at the front.

b. ENABLE
Locate the hole which gives access to the PRE-CAL ENABLE switch.

Insert an insulated tool in the hole and move the pre-cal switch to the right (Enable).

The legend 'cal', as presented on the MODE display, also appears on the OUTPUT display.

Caution! The following operation (c) clears all the calibration memory stores as part of pre-calibration. Proceed only if this is required.

c. CLEAR
Locate the hole which gives access to the Calibration Memory CLEAR push-button.

Insert an insulated tool in the hole and press the button to clear the calibration memory.
Refit the top cover but do not secure.

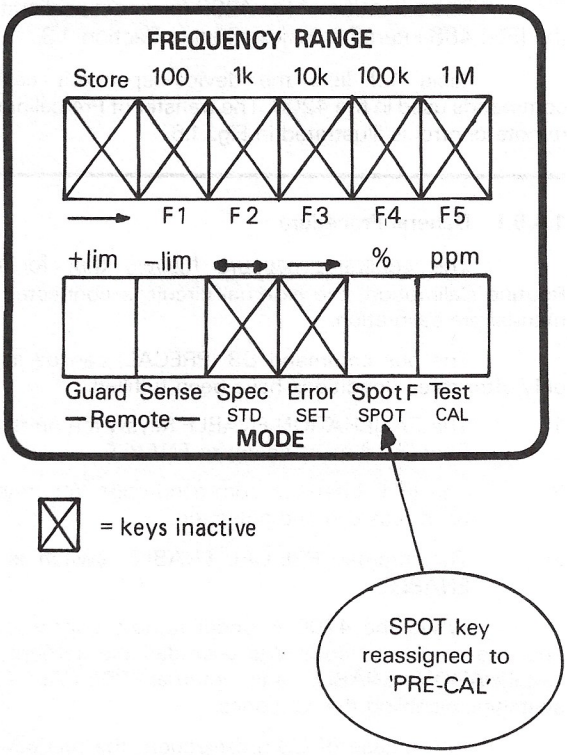


FIG. 1.5 PRECALIBRATION – USE OF MANUAL KEYS

1.4.4.2 Setting the Pre-cal Parameters

a. IVD
Select x1.0 ratio.

b. 4200
Select 10V range, at 1kHz on the 1kHz Frequency range.
Select 1.000,00V.
Press the SPOT key, its LED lights.
Use 4200 OUTPUT ↑|↓ keys to adjust the DVM reading to 1V.
Press CAL: the SPOT LED remains lit.

c. IVD
Select the x0.1 ratio to divide the 4200 output by 10.

d. 4200
Select Full Range.
Use 4200 OUTPUT ↑|↓ keys to adjust the DVM reading to 1V.
Press the CAL key; the SPOT LED goes OFF and display reverts to nominal 10V. Pre-cal is now completed.

Select OUTPUT OFF and disconnect.

1.4.4.3 4200 PRE-CAL ENABLE Switch

CAUTION! **DO NOT** press the internal push-button which clears the calibration memory. If this is done, any parameters stored in the calibration memory are cleared; so pre-calibration in cancelled, and must be repeated.

a. Cover
Lift the top cover at the front.

b. Locate
Locate the hole which gives access to the PRE-CAL ENABLE switch.

c. Disable
Insert an insulated tool in the hole Pre-cal and move the switch to the left (RUN).

d. Display
The legend 'cal' remains on the MODE display, but disappears from the OUTPUT display.

e. Cover
Refit and secure the top cover.

1.4.5 Remote Pre-Calibration Guidelines

The operation of the 4200 for remote calibration via the IEEE 488 interface, is described in Section 1.3.

Table 1.2 lists the device-dependent calibration commands used in the 4200. The transfer of Pre-calibration to remote control is illustrated in Fig. 1.6.

1.4.5.1 General Procedure

The general procedure follows that for remote Routine Calibration; the external circuit is connected as for manual pre-calibration.

The bus command C3 (PRECAL) can be activated only after three conditions have been fulfilled:

1. The CALIBRATION ENABLE Keyswitch on the 4200 Rear Panel must be set to ENABLE,
2. The IEEE Interface command-code W1 must have been received and activated.
3. The internal 'PRE-CAL ENABLE' switch is set to ENABLE.

When the 4200 is under remote control over the bus, the command code WØ overrides the settings of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

In the case of C3 preselection, the procedure is in two stages, so a first transmission of CØ merely transfers to the second stage. The second CØ transmission cancels the preselected mode.

For C3, the CPU uses the value input by 'M' Code to distinguish between Full Range or 10% of Full Range gain calibration.

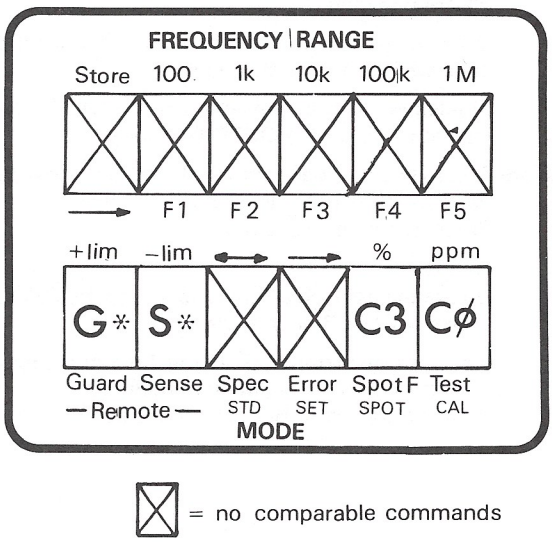


FIG. 1.6 TRANSFER OF PRECALIBRATION TO REMOTE CONTROL

1.4.5.2 Pre-Calibration Command Strings

The following six command strings are given for the sole purpose of illustrating the methodology for the remote pre-calibration mode. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the 4200 has previously been programmed into the 10V range at a frequency in the LF band (refer to the User's Handbook Section 8, Page 8-2), and that the external circuit is set up correctly.

The 4200 has already been programmed into its calibration mode by W1, with the calibration keyswitch and the internal PRE-CAL ENABLE switch set to ENABLE.

The calibration memory stores have been cleared, and the 4200 Output is OFF.

The string sequence for pre-calibration is as follows:

H	(LF)
C3	(automatically sets nominal Full Range)
O1	(Output On)
=	
M***	(adjust for null at Full Range)
=	
CØ	(executes the first-stage calibration)
=	
M***	(adjust for null at 10% Full Range)
=	
CØ	(executes the second-stage calibration)
=	
OØ	(Output Off)
=	

The precalibration should be terminated as detailed in para 1.4.4.3.

SECTION 2

FAULT DIAGNOSIS

WARNING **HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.**
ELECTRIC SHOCK CAN KILL

CAUTION The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

2.1 INTRODUCTION

2.1.1 Use of Diagnostic Guides

The diagnostic guides given in Section 2.2 are intended to aid the user in locating a failed printed circuit board or other assembly. The self-diagnostic capabilities of the 4200 provide the first step in fault analysis by displaying a FAIL message on the mode display. Initial actions to be taken after the occurrence of a FAIL message are given, where applicable, in the diagnostic guides of Section 2.2. The FAIL message localizes the failure into a distinct functional area and the "Fault Condition" summary in each guide relates the function failure to a probable hardware boundary.

The identities of the assemblies involved in the failure are given beneath the fault condition summary, but it is unlikely that all assemblies listed will prove to be faulty. For successful failure analysis, it is advisable to be familiar with the electronic functioning of the instrument and with the physical location of the assemblies. To assist in these aspects, the diagnostic guides include references to relevant parts of this publication.

2.1.2 Effects of Protective Measures on Diagnosis

2.1.2.1 Protective Suppression of Fault Conditions

The 4200 incorporates built-in protection in hardware and software. To minimize damage, protective circuitry acts immediately, backed up by a pre-programmed CPU response to detected failure symptoms. The CPU informs the user by presenting a failure message on the MODE display.

When investigating a failure, it should therefore be anticipated that protective measures will have suppressed the original fault conditions. A useful starting-point is to identify the origin of the failure message to localize the area of search.

2.1.2.2 FAIL 5 as Default State

Faults which result in display messages FAIL 2, 3 or 4 can pose a safety hazard to the operator, and apply excessive voltage to external circuitry. To protect against this, the instrument is programmed to default to FAIL 5 state as rapidly as possible after its initial response to the failure symptoms. The CPU switches Output OFF and trips the safety monitor (Watchdog). If the conditions of the original failure message have been removed the display changes to FAIL 5.

In normal use, an operator will probably notice only FAIL 5, and miss the original failure message. In FAIL 5 state, front panel control is inhibited until Safety Reset is pressed. This returns the instrument to the state for which the original fault conditions and failure message were produced, but with Output OFF.

2.1.2.3 To Observe the Original Failure Message

Two procedures can be used:

(a) Carry out the self-test routine of Section 2.3. The failure message may recur during this test.

(b) Reset the instrument to reproduce the fault, carefully watching the MODE display. The original failure message should reappear momentarily, prior to defaulting into FAIL 5.

Then select the appropriate diagnostic guide in Section 2.2.

2.2.1 FAIL 1 Display Message

DISPLAY: FAIL 1

Excessive Internal Temperature

INITIAL ACTION

1. Switch Power OFF.
2. Allow to cool for 15 minutes.
3. Switch Power ON—If FAIL 1 persists, repeat 1 & 2.
4. Select operating mode when FAIL 1 clears.
5. No failure display—no further action.
   FAIL 1 recurs —fault persists.

FAULT CONDITION

High temperature sensed in:

1. Positive Heatsink Assembly

   or

2. Negative Heatsink Assembly

Fault indication signal OVERTEMP active.

POSSIBLE FAULT LOCATION

1.	Positive Heatsink Assembly	400538
2.	Negative Heatsink Assembly	400539
3.	Power Amplifier Assembly	400450

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.13, 7.9.
Technical descriptions: Section 4.12

2.2.2 FAIL 2 Display Message

DISPLAY: FAIL 2

Over-Voltage

INITIAL ACTION

N.B. This failure can be caused by injection of an external voltage across the 4200 terminals. The trip level is between 75V and 110V RMS.

1. Ensure that OUTPUT IS OFF (4200 should have tripped to FAIL 5).
2. Disconnect external leads from 4200 terminals.
3. Press Safety Reset.
4. Carry out self-test sequence.
5. FAIL 2 recurs—fault persists.
6. No failure display—Reproduce original conditions in Local Sense with no external connections.
7. No failure display—check external circuit and proceed with careful use.
8. FAIL 2 recurs—fault persists.

FAULT CONDITION

1. Over voltage circuit on the Output Control Assembly has detected the excess voltage at between 75V and 110V RMS between PHi and PLo lines, and has activated $\overline{\text{HV ST}}$ signal to the CPU AND
2. The CPU has recognized that the instrument is not in High Voltage State, so has generated FAIL 2 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1.	Injection of external voltage	
2.	Output Control Assembly	400550
3.	Power Amplifier Assembly	400450

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.5, 7.9.
Self-test procedure: Section 2.3.
Technical descriptions: Section 4.12.

2.2.3 FAIL 3 Display Message

DISPLAY: FAIL 3

Control Data Corrupted.

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Control data corrupted.
2. CPU has detected errors in serial transfer of data between out-guard and in-guard circuits, and generated FAIL 3 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

1.	Reference Divider Assembly	400535
2.	Analog Interface Assembly	400570

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.4, 7.3.

Technical descriptions: Section 4.5.

2.2.4 FAIL 4 Display Message

DISPLAY: FAIL 4

Precision Divider Fault.

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Precision divider fault.
2. CPU has detected errors in the most-significant data bits set in the precision divider input data latches, and generated FAIL 4 display. THEN
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

Analog Interface Assembly	400570

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.3.

Technical description: Section 4.6.

2.2.5 FAIL 5 Display Message

DISPLAY: FAIL 5

Safety Monitor (Watchdog) Tripped.

INITIAL ACTION

Use the checking sequence below, watching the MODE display carefully at each stage to detect any FAIL number appearing momentarily before FAIL 5. If no failure message occurs, carry on to the next stage.

Stage 1: Press Safety Reset.

Stage 2: Carry out self-test sequence (Section 2.3).

Stage 3: Set Output ON.

Stage 4: Proceed with careful use.

If FAIL 2 occurs at stage 3, ensure that it is not due to injection of an excessive external voltage by disconnecting the 4200 terminals and repeating the checks. If FAIL 5 alone occurs, proceed to "Fault Condition" below. For any FAIL other than FAIL 5, transfer to the diagnostic guide for that message.

FAULT CONDITION

18mS monostable (M10 in reference divider) has been deprived of at least two trigger pulses and has timed out, activating "BARK" and "BARK DELAYED" (BARK+47mS) signals from M13 in the reference divider pcb.

Summary of "BARK" effects:

1. Removes the drive from the High Voltage (1kV) transformer.
2. $\overline{\text{BARK DELAYED}}$ Disables the 400V Power Supply.
3. Status message sent to CPU signalling a failure.
4. CPU starts controlled shut-down.

Summary of "BARK DELAYED" effects:

1. Disconnects the AC voltage Power and Sense circuits from the instrument output terminals.
2. Disables the registers of the serial/parallel data converters.
3. Outputs from control latches in the reference divider pcb are disabled by setting into "Tristate". Each output line has a pull-up or pull-down resistor which sets the analog circuitry into a safe condition.

POSSIBLE FAULT LOCATION

1. Digital Assembly (No gated WRT STRB pulses at J2/J3-29) 400534
2. Analog Interface Assembly (No SSDA strobe pulses; or Watchdog disabled) 400570
3. Reference Divider Assembly (Incorrect functioning of Watchdog setup circuitry) 400535

N.B. The Watchdog is designed primarily to ensure that CPU malfunctions do not set up dangerous conditions in the analogy circuitry.

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.2, 7.3, 7.4.

Technical description: Section 4.5.

2.2.6 FAIL 6 Display Message

DISPLAY: FAIL 6

Calibration Memory Fault.

INITIAL ACTION

1. Select Output OFF, Spec OFF, Error OFF.
2. Perform self-test sequence (Section 2.3).
3. No failure display—no further action.
4. FAIL 6 recurs—recalibration required.
5. Select Cal
6. Recalibrate

} Refer to Section 1.

7. Calibration failure—fault persists.

FAULT CONDITION

Calibration memory fault on Digital pcb assembly.

POSSIBLE FAULT LOCATION

Digital Assembly	400534

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.2.

Self-test procedures: Section 2.3.

Calibration procedures: Section 1.

Technical descriptions: Section 4.2.

2.2.7 FAIL 7 Display Message

DISPLAY: FAIL 7

P.A. 400V Power Failure

INITIAL ACTION

1. Switch Power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power ON—no failure display—no further action.
4. FAIL 7 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 400V power supply failure.
2. Fault indication signal 400V(2) FAIL active.
3. Check line input voltage.
4. It is possible for a misleading FAIL 7 message to occur, caused by a logic supply failure in particular −15 Volts. Refer for fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Positive Heatsink Assembly	400538
4.	Negative Heatsink Assembly	400539
5.	Power Supply/I Heatsink Assembly	400540
6.	Mother Board	400532

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.9, 7.4, 7.13, 7.16.

Technical descriptions: Sections 4.12 and 4.16.

2.2.8 FAIL 8 Display Message

DISPLAY: FAIL 8

P.A. 38V Power Failure.

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on—no failure display—no further action.
4. FAIL 8 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 38V power supply failure.
2. Fault indication signal 38V(2) FAIL active.
3. Check line input voltage.
4. It is possible for a misleading FAIL 8 message to occur, caused by a logic supply failure, in particular −15 Volts. Refer to fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Power Supplies	400544
4.	Mother Board	400532

FURTHER INFORMATION IN THIS HANDBOOK

Page number: 7.9, 7.4, 7.12, 7.16.
Technical descriptions: Section 4.16.

2.2.9 FAIL 9 Display Message

DISPLAY: FAIL

P.A. 15V Power Failure

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on—no failure display—no further action.
4. FAIL 9 recurs—fault persists.

FAULT CONDITION

1. Positive or Negative 15V power supply failure.
2. Fault indication signal 15V(2) FAIL active.
3. Also 400V power supply is disabled.
4. Check line input voltage.

POSSIBLE FAULT LOCATIONS

1.	Power Amplifier Assembly	400450
2.	Reference Divider Assembly	400535
3.	Power Supplies	400554

FURTHER INFORMATION IN THIS HANBOOK

Page number: 7.9, 7.4, 7.11.
Technical descriptions: Section 4.16.

2.2.10 Error OL Display Message

DISPLAY: ERROR OL

AC Volts: Output current limit exceeded.

Current: Output compliance voltage limit exceeded.

INITIAL ACTION

1. If AC Voltage range selected:
   (a) Set Output OFF (automatic if 100 or 1000V range selected).
   (b) Disconnect external circuit.
   (c) Set Output ON:
   — If no Error OL or FAIL message, check external circuit for low resistance, drawing output current in excess of specification (Table 2.1). Ensure Capacitive Load constraints are not exceeded, refer to User's Handbook Section 6 page 6.5.
   — If Error OL recurs, internal fault persists.

2. If I range selected:
   (a) Set Output OFF.
   (b) Short Output terminals I+ to I−.
   (c) Set Output ON:
   — If no Error OL or FAIL message, check external circuit for high resistance, developing output voltage in excess of 3V compliance limit.
   — If Error OL recurs, internal fault persists.

OUTPUT CURRENT LIMIT	OUTPUT RANGE	FREQUENCY RANGE
25mA	1V	All Ranges
60mA	10V	All Ranges
120mA	100V	All Ranges
15mA	1kV	100Hz/1kHz
65mA	1kV	10kHz/100kHz/1MHz

FAULT CONDITION

1. If 1mV, 10mV, 100mV or IV range:
   Sine Source Assembly overcurrent sense circuit (M49a/M49b) has detected a current in the AC 1V line of approximately 25mA RMS or more, and has activated $\overline{\text{LIM ST}}$ signal to the CPU.

2. If 10V range:
   10V overload detector in the Power Amplifier Assembly has detected a current in the I+ line of approximately 60mA RMS or more. In this condition a hardware limit comes into effect.

3. If High Voltage ranges (100V or 1kV):
   Either
   (a) 100V Overload detector in the Power Amplifier Assembly has detected a load in excess of 120mA RMS on the 400V power supply,
   (b) 1kV Current Overload detector (M8) in the Output Control assembly has detected an excessive output current,
   or
   (c) 1kV Overvoltage Detector in the Output Control Assembly has detected a voltage on the PHI(V) line in excess of 1440V RMS.
   In these ranges the output is switched off automatically by the CPU.

4. If I range selected:
   Overvoltage detector circuit has detected a terminal voltage of 3V RMS or more and has activated $\overline{\text{LIM ST}}$ signal to the CPU. If 100mA or 1A range selected, the CPU switches Output OFF.

POSSIBLE FAULT LOCATIONS

1. External circuit
2. Sine Source Assembly 400446
3. AC Assembly 400447
4. Output Control Assembly 400550
5. Power Amplifier Assembly 400450
6. IAssembly 400555

FURTHER INFORMATION IN THIS HANDBOOK

Page numbers: 7.6, 7.7, 7.5, 7.9, 7.8.

Technical descriptions:

Low AC Voltage ranges: Section 4.11.

100 or 1000V ranges: Section 4.12.

I ranges: Section 4.15.

2.3 SELF-TEST SEQUENCE

2.3.1 General

The self-test sequence is performed in two stages:

Stage 1 is a fully automated test of safety monitoring and high-voltage safety interlocks;

Stage 2 is a semi-automatic test of keyboard and display functions, which also responds to operator's key selections.

2.3.2 Stage 1 (Fig. 2.1)

Entry into Stage 1 is selected automatically whenever the TEST key is pressed for the first time (the test is not allowed if OUTPUT ON, ERROR or SPEC are selected or when in remote control).

Indication of test mode is given by the LED in the TEST key being lit. The full sequence of Stage 1 must be completed before exit from the test mode can be made. The tests performed in Stage 1 are as follows:

1. Safety Monitor Watchdog Test. In this, the safety monitor is tripped causing the word SAFEtY to appear in the Mode display, the Safety Reset LED flashes and the buzzer sounds continuously. It is necessary for the operator to reset the safety monitor by pressing the Safety Reset key, after which the SAFEtY display is replaced by the 'running' message, and the test sequence continues.
2. Calibration Memory Test. The contents of the non-volatile calibration RAM are checked for validity. Failure results in the message FAIL 6 appearing on the Mode display.
3. High-voltage Protection. This test ensures that a voltage demand made to the power amplifier does not trip the software voltage detector when immediately below the detector threshold level, but when raised to a level above the detector threshold the detector is tripped.

   Incorrect detect action is shown by the message FAIL 2 on the Mode display. No voltages appear at the output terminals during this test.

   Fail messages are updated as the test sequence progresses through the calibration memory and high-voltage tests.

   After completion of the high-voltage test, the test mode ends and the Test LED is cancelled. If faults were encountered the last FAIL message will remain on the display replacing the running message. Fault diagnosis can now be performed. If no faults are encountered during Stage 1, the message PASS is displayed. The calibrator can now be returned to normal operation, or Stage 2 of the self-test sequence can be selected.

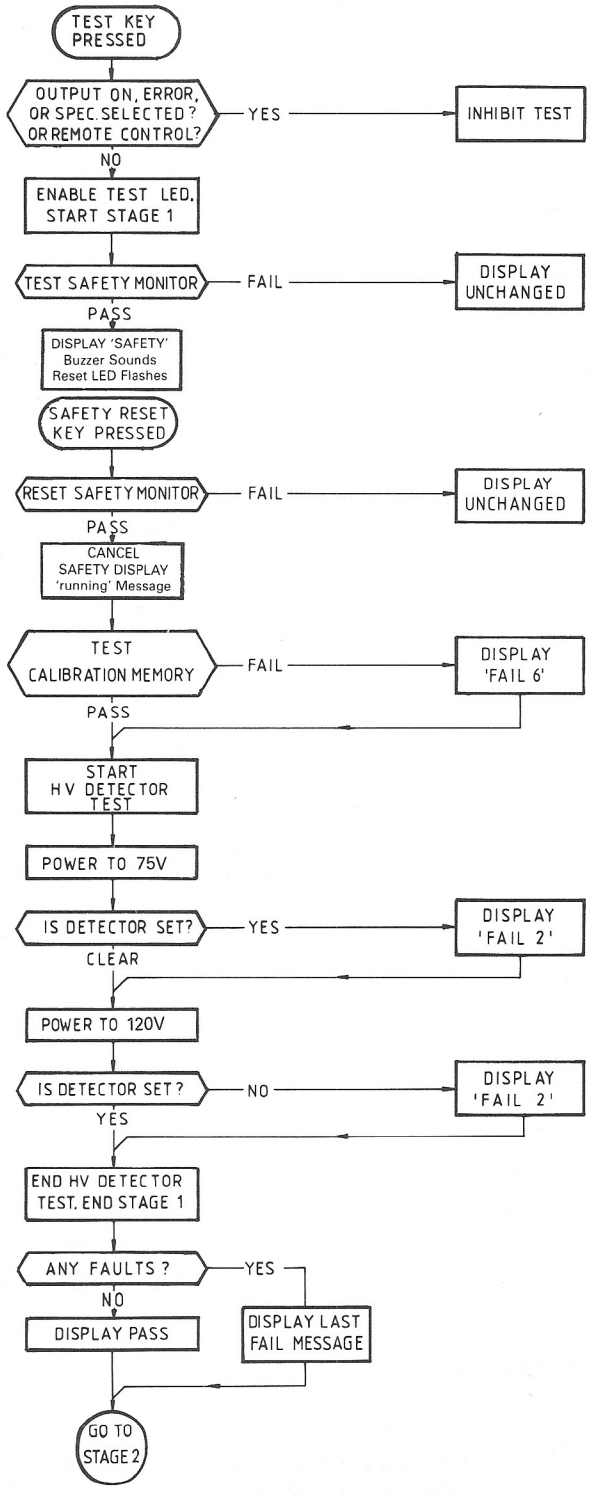


FIG. 2.1 SELF TEST SEQUENCE STAGE 1

2.3.3 Stage 2 (Fig. 2.2)

Entry into Stage 2 of the self-test sequence is made when the Test key is pressed AFTER the completion of Stage 1. The test proceeds by sequentially displaying all segments and legends.

The test continues, showing segment-by-segment, all seven-segment digits, legends and commas.

After all digits have been displayed, the keyboard LED indicators are lit in a sequence which proceeds from left to right. (Test LED remains lit).

The next test in the sequence requires operator participation in order to check key functions. Two half-digit symbols are shown on the mode display to indicate that the keys are ready to be checked.

Operation of Up, Down and Output Selection keys are shown by a symbol on the display immediately above the key; operation of Frequency Range, Mode, Range, Function and Output keys are shown by the key's LED. In these tests the display or LED remains lit until another key is pressed.

At any part of Stage 2, pressing Test or Zero key will end the test and cancel the Test LED.

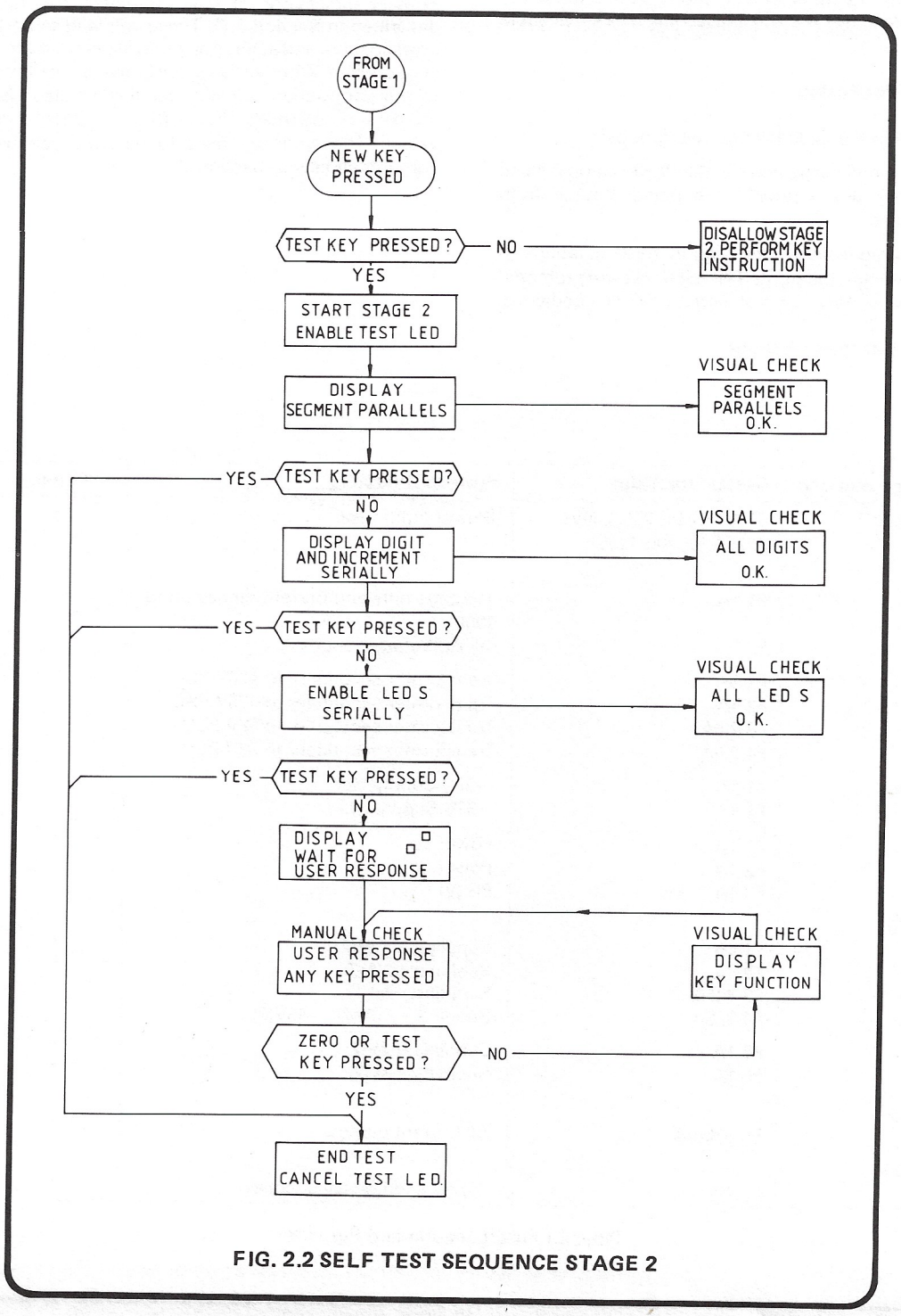


FIG. 2.2 SELF TEST SEQUENCE STAGE 2

2.4 Fuse Protection

In addition to the electronic protection devices used in the 4200, fuses are provided to protect against catastrophic component failure.

2.4.1 Fuse Replacement

A blown fuse is merely a symptom of failure, in the large majority of cases the cause lies elsewhere.

CAUTION Every occurrence of a blown fuse should be investigated to find the cause. Only when satisfied that the cause is known, and has been removed, should a user replace a fused link by a serviceable item.

2.4.2 Reasons For Fusing

The fuses in the 4200 fall into two groups:

i) Clip-in anti-surge fuses in the Power Supplies and Mother Board protect the power source from damage.

ii) Soldered-in fuses are used in some locations to ensure that the printed circuit tracks are protected in the unlikely event of extreme failure conditions.

Table 2.1 lists their locations.

2.4.3 Locating a Blown Fuse

The ultimate causes of blown fuses are so extensive that it is impractical to list them. In many cases the underlying cause, or the blown fuse itself, will activate an electronic protective process which can conceal some of the symptoms.

Fault location in the 4200 should proceed from the primary indications of fault condition (e.g. failure messages described in Section 2.2). These will lead to particular areas of investigation, and at this point the relevant circuit fuses should be checked first. Whether fuses are blown or not, the checks will add to the information available for further diagnosis. Table 2.1 is indexed in Assembly Circuit Diagram page order, giving fuse values. The types of fuses to be used can be found in the component lists of Section 6.

Location and Page numbers	Designator/Value	Protected Circuits	Clip-in	Solder-in
Power Input Module Page 7.18-6 (15)	F1 (3.15A for 220/240V) (6.25A for 100/120V)	(Power Input fuse)	*	
AC Assembly Page 7.7-1	F1 1A	1V range only and Current ranges up to 10mA		*
	F2 1A	All AC Voltage ranges		*
Mother Board Page 7.16-5	F1 1A	Transformer secondary to 400V PSU	*	
	F2 1A	Transformer secondary to 400V PSU	*	
	F3 2.5A	Transformer secondary to 38V PSU		*
	F4 2.5A	Transformer secondary to 38V PSU		*
Power Supply (38V) Page 7.12-1	F1 1A	—38V Supply Line		*
	F2 1A	+38V Supply Line		*
Output Control Page 7.5-1	F1 1A	Power Lo		*
	F2 1A	Power Lo		*
	F3 1A	PHI(V)		*
Power Supply (IG) Page 7.11-1	F1 4A	Supplies —22V(2)	*	
	F2 4A	Supplies +22V(2)	*	
	F3 3.15A	Supplies +15V(2)	*	
	F4 3.15A	Supplies —10V(2), —15V(2)	*	
Page 7.11-2	F5 1A	Supplies —8V(2)	*	
	F6 1A	Supplies +8V(2)	*	
Current Assembly Page 7.8-1	F5 375mA	All Current outputs		*
Power Supply (OG) Page 7.10-1	F1 4A	Digital and Display supplies	*	

Table 2.1 Fuse Location and Purpose

SECTION 3

DISMANTLING AND REASSEMBLY

3.1 GENERAL PRECAUTIONS

3.1.1 WARNINGS

(1) **ISOLATE THE INSTRUMENT FROM POWER SUPPLIES BEFORE DISMANTLING OR REASSEMBLING.**

(2) **THE COMBINED REMOVAL OF TOP AND BOTTOM COVERS, GROUND/GUARD ASSEMBLIES AND REAR PANEL ASSEMBLY; LEAVES THE MOULDED INTERNAL CHASSIS UNSUPPORTED. THIS CAN CONSTITUTE A SAFETY HAZARD TO BOTH PERSONNEL AND EQUIPMENT.**

3.1.2 CAUTIONS

(1) Removal of the Top Ground/Guard Assembly invalidates the manufacturers calibration certification.

(2) Handle the instrument carefully, especially when inverted, to avoid shaking printed circuit boards loose.

(3) Do not touch the pcb edge connectors with the hands.

(4) Ensure that no wires are trapped when fitting ground/guard assemblies.

(5) Ensure that washers, nuts etc. do not fall into the instrument, and are correctly refitted at subsequent reassembly.

3.2 General Mechanical Layout

The 4200 AUTOCAL STANDARD can be used as a benchtop instrument, or it may be rack mounted in a standard 19" rack. All circuits are housed within a single unit on printed circuit board assemblies, the eight major PCBs being plugged into a "Mother" PCB assembly.

A labelled view of the open instrument is shown in Volume 2 (page 7.0-1). Exploded views are shown on pages 7.18-1 to 7.18-6.

3.2.1 Front Panel

Six output terminals with captive, insulated caps are provided. Alternatively, the terminals can be fitted to the rear panel (Option 42) at manufacture.

A printed overlay on the front panel labels all the controls, and retains polarizing filters for the displays.

3.2.2 Rear Panel

The recessed Power Input plug, Power Fuses and Line Voltage Selector are contained in an integral filter module at the centre of the rear panel.

The Calibration Enable switch (with removable key), and the External Reset socket (J53) are mounted directly on the panel between the Power Input module and the cooling-air intake filter.

The intake filter is retained by a grille but is removable for cleaning. At the extreme left of the panel, an extractor fan draws cooling air through the filter and internal heat exchangers, discharging to atmosphere.

The IEEE 488 standard connector socket (J27) with instrument address switch, the Calibration Interval Switch and switch S53 (not used on the 4200); are all mounted on the Interconnection PCB assembly. This is fitted on spacers to the inside face of the panel with external components protruding to the rear.

3.3 LOCATION AND ACCESS

3.3.1 External Construction

Rigid side extrusions, together with the front and rear panel assemblies, form the basic chassis of the instrument. The side extrusions have handles and rear spacers fitted for bench-top use, or are fitted with 'ears' and slides for rack mounting (see User's Handbook, Section 2).

The top cover locates into the side extrusions and is secured by screws. The bottom cover is attached in the same way, and includes six domed feet. An operator's instruction card pulls forward from below.

3.3.2 Internal Construction

The chassis is enclosed top and bottom by ground and guard screens. The upper ground and guard screens allow most internal adjustments to be performed without removal. Locations of adjustable components, instructions and warnings are printed on its upper surface.

The interior of the chassis is divided into two compartments. A thermally-enclosed compartment occupies the forward half of the chassis, and is used to house the low power, precision printed circuit board assemblies.

The rear compartment contains high power components, is air-cooled and further subdivided. One section is positioned across the intake airflow, housing the In-guard and Out-guard Power Supply assemblies and providing anchorage for the Mains (Line) Transformer assembly. The other section houses three Heatsink assemblies, provides anchorage for the LF Transformer assembly, High Voltage assembly and 38V Power Supply assembly.

Filtered air passes over the power supplies, mixes with air in the rear copartment, is drawn through the heatsink assemblies, and is finally expelled from the instrument by the extractor fan.

Guard screens are provided against the outer walls of the power supply sub-compartment and the heat-sink compartment.

Interconnections between the Power Amplifier assembly, all forward-compartment assemblies, and the Front assembly are made via a Mother PCB. The latter fits across the bottom of the forward compartment, extending at the front to the Front assembly and at the rear to the 38V Power Supply. Four moulded stiffeners keep the mother pcb rigid, also providing lateral locating slots for printed circuit boards and guard screens.

The main printed circuit boards in the forward compartment fit across the full width of the instrument chassis. They slide into vertical slots cut into the moulded chassis, their PCB edge-connection fingers making electrical contacts with sockets mounted on the Mother Assembly. Interleaved between the assemblies are screening shields. These are also guided by slots, and make similar electrical contact.

The Power Amplifier assembly PCB slots in behind the forward compartment across the full width. It connects to the Mother PCB in the same way, but has additional discrete electrical connections for the high power lines.

Each PCB is identified by the color of its ejector lever. The color name is coded at the correct location on the top of the internal moulded chassis (refer to Table 3.1). Also, each assembly's edge connector is uniquely configured to prevent incorrect fitting.

The Front PCB assembly, carrying the display components, connects into the front end of the mother PCB outside the thermally-insulated compartment.

3.4 GENERAL ACCESS

ENSURE THAT POWER IS OFF.
Heed the Warnings and cautions 3.1.1 & 3.1.2.

If, during a procedure, sufficient access has been obtained then no further dismantling is required.

3.4.1 TOP COVER REMOVAL
(7.18-2 Details 11)

a. Remove the eight M4×12mm socket head countersunk screws from cover.
b. Remove cover by lifting at the front.

3.4.2 TOP COVER FITTING

Locate cover at rear first, then reverse procedure of para. 3.4.1.

3.4.3 BOTTOM COVER REMOVAL
(7.18-2 Detail 11)

a. Invert the instrument.
b. Remove the eight M4×12mm socket head countersunk screws from cover.
c. Remove cover by lifting at the front.

3.4.4 BOTTOM COVER FITTING

Locate cover at rear first, then reverse procedure of para. 3.4.3.

3.4.5 FRONT PANEL—REMOVAL
(7.18-4 Detail 6)

a. Remove the four M4×8mm taptite screws from the front panel.
d. Remove the Front Panel.

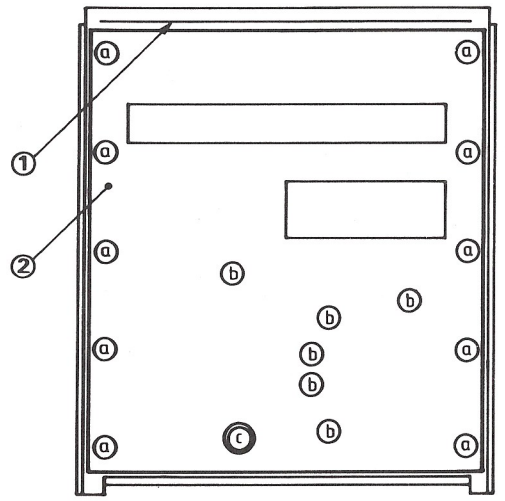
3.4.6 FRONT PANEL—FITTING

Reverse the procedure of para. 3.4.5, referring to Page 7.18-4.

TABLE 3.1 INTERNAL LOCATION AND ACCESS
(Top Cover and Top Ground/Guard assembly removed)

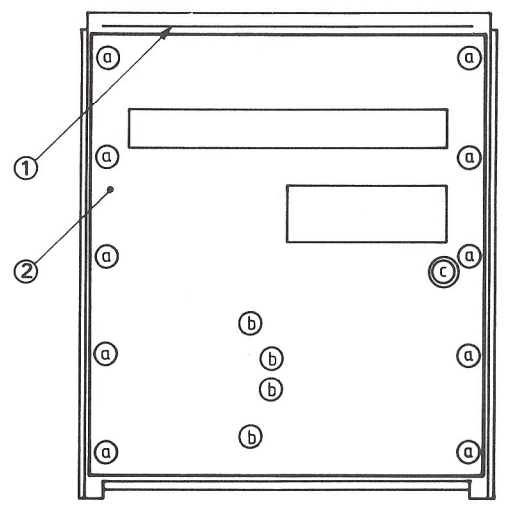
Note:
Unless removing the Instruction Card or the Rear Panel only; remove the Top Cover: Sub-section 3.4.1.
In addition to the following Location instructions, refer to Volume 2 page 7.0-1.

Assembly	Access Required (Heed Caution 3.1)	Location (Page Detail in bracket)	Ejector Color	Section	Page (Volume 2)
Instruction Card	—	7.18-2 (12) —	—	3.5.1	—
Front Assembly	3.4.3 & 3.4.5		—	3.5.2	7.1-1
Digital Analog Interface Reference Divider Output Control Sine Source AC Current (OR Current Link pcb)	3.4.7	Chassis Identifier Code BLK BRN RED ORG YEL GRN BLU BLU	BLACK BROWN RED ORANGE YELLOW GREEN BLUE BLUE	3.5.4	7.2-1 7.3-1 7.4-1 7.5-1 7.6-1 7.7-1 7.8-1
Common Guard and Ground Screens	3.4.7	7.18-5 (13) —	—	3.5.6	—
Power Amplifier	3.4.7	7.18-1 (4) VLT	VIOLET	3.5.8	7.9-1
Power Supplies Out-Guard In-Guard ±38V	3.4.7	7.18-1 (1) — 7.18-1 (2) — 7.18-1 (5) —	— — —	3.5.10 3.5.12 3.5.14	7.10-1 7.11-1 7.12-1
Heatsinks	3.4.7	7.18-1 (4) —	—	3.5.16	7.13-1
High Voltage	3.4.7	7.18-1 (5) —		3.5.18	7.14-1
Transformers Mains HF LF	3.4.7	7.18-5 (9) — 7.18-4 (6) — 7.18-5 (10) —	— — —	3.5.20 3.5.22 3.5.24	— — —
Mother Board	—	7.18-3 (3) —	—	—	7.16-1
Interconnection Board	3.5.28	7.18-6 (15) —	—	—	7.17-2
Terminal Board	3.4.5	7.18-4 (8) —	—	3.5.26	7.17-3
Rear Panel	—	7.18-4 (6) —	—	3.5.28	7.18-6



1. FRONT PANEL ASSEMBLY
2. TOP GROUND/GUARD ASSEMBLY

FIG. 3.4.1 FITTING TOP GROUND/GUARD



1. FRONT PANEL ASSEMBLY
2. BOTTOM GROUND/GUARD ASSEMBLY

FIG. 3.4.2 FITTING BOTTOM GROUND/GUARD

3.4.7 TOP GROUND/GUARD ASSEMBLY REMOVAL
(Fig. 3.4.1)

CAUTION

Before proceeding it must be noted that removal of the Top ground/guard shield involves breaking Datrons calibration seal and renders manufacturers calibration invalid.

Access

Remove the top cover (para. 3.4.1).

a. Refer to Fig. 3.4.1 and remove:
   1. from position 'a', ten M4×8mm pozi-countersunk screws;
   2. from position 'b', six M3×6mm pozi-pan screws and M3 shakeproof washers;
   3. from position 'c', one M3×12mm pozi-pan screw and M3 shakeproof washer.

b. Remove the top ground/guard assembly.

3.4.8 TOP GROUND/GUARD ASSEMBLY FITTING

Reverse the procedure of para. 3.4.7.

3.4.9 BOTTOM GROUND SHEET ASSEMBLY—REMOVAL
(Fig. 3.4.2)

Access

Invert the instrument.
Remove the bottom cover (para 3.4.3).

a. Refer to Fig. 3.4.2 and remove:
   1. from positions 'a', ten M4×8mm pozi-countersunk screws;
   2. from positions 'b', four M3×6mm pozi-pan screws and M3 shakeproof washers;
   3. from position 'c', one M3×12mm pozi-pan screw and M3 shakeproof washer.

b. Remove the bottom ground sheet assembly.

3.4.10 BOTTOM GROUND SHEET ASSEMBLY—FITTING

Reverse the procedure of para. 3.4.9.

3.4.11 BOTTOM GUARD PLATE—REMOVAL
(Page 7.18-1 Detail 8)

Access

Invert the instrument.
Remove the bottom cover (para. 3.4.3).
Remove the bottom ground sheet assembly (para. 3.4.9).

a. Refer to Page 7.18-1 Detail 8 and remove nine M3×6mm pozi-countersunk screws.

b. Remove the bottom guard plate.

3.4.12 BOTTOM GUARD PLATE—FITTING

Reverse the procedure of para. 3.4.11 ensuring that no wiring is strained or trapped.

3.5 REMOVAL AND FITTING

3.5.1 INSTRUCTION CARD

a. Pull the instrument card forward to its fullest extent.

b. Bow the card and release the rear lugs from the slots.

c. Refit in reverse procedure.

3.5.2 FRONT ASSEMBLY—REMOVAL
(Page 7.18-3 Detail 4)

a. Remove two screws retaining the power switch, together with their two shakeproof washers and four plain washers.

b. Fold the power switch and its cable clear of the pcb.

c. Remove the M3×6mm pozi-pan screws from 13 positions on the circuit board.

d. Ease the lower edge of the PCB away from the Mother PCB, to disengage the mating connectors. Remove two M2.5×10mm pozi-pan screws and disconnect the power Switch (Page 7.18-3 Detail 4).

e. Remove the assembly.

3.5.3 FRONT ASSEMBLY—FITTING

Reverse the procedure of para. 3.5.2. Ensure all mating connectors are fully engaged and that the surfaces of displays are clean.

3.5.16 HEATSINK ASSEMBLIES—REMOVAL
(Page 7.18-5 Detail 12)

Heed the Warnings and Cautions 3.1.1 & 3.1.2.

a. Remove the six M3×12mm pozi-countersunk screws from the heatsink retaining plate.

b. Remove the heatsink retaining plate.

CAUTION
Allow heatsinks to cool before handling.
Do not pull on the connector wires.

Note:
Although the heatsink assemblies are discrete items, removal is simplified when performed in the following order:

1. Negative Heatsink assembly;
2. Positive Heatsink assembly;
3. Power Supply/Current Heatsink assembly.

When disconnecting connectors, some resistance to movement will be felt from the locking clips of the connector bases.

c. Disconnect connectors at the following points:
J1—Positive Heatsink assembly.
J2—Power Amplifier assembly.

d. Remove Negative Heatsink assembly.

e. Disconnect J3 at the Power Amplifier assembly.

f. Remove the Positive Heatsink assembly.

g. Disconnect at the following points:

Connector	Assembly
J1	Power Amplifier Assembly
J31, J19	Mother Assembly
J1	In-Guard PSU Assembly

h. Remove the Power Supply/Current Heatsink assembly.

3.5.17 HEATSINK ASSEMBLY—FITTING

Reverse procedure of para. 3.5.16.

To ensure correct location, orient the PCB side of each heatsink to face inwards.

3.5.18 HIGH VOLTAGE ASSEMBLY—REMOVAL
(Page 7.18-1 Detail 5)

a. Lift the assembly upwards as shown on Page 7.18-1 Detail 5.

b. Remove the connections J2, J3 and J4, shown in the diagram.

c. Lift the assembly clear of the instrument.

3.5.19 HIGH VOLTAGE ASSEMBLY—FITTING

Reverse the procedure of para. 3.5.18 referring to Page 7.18-1 Detail 5.

3.5.20 MAINS TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-5 Detail 9)

a. Remove the Out-Guard and In-Guard Power Supply assemblies (see paras 3.5.10 and 3.5.12).

b. Disconnect the connectors from the transformer at the following assemblies:

J32 — Mother Assembly
J6 — Interconnection Assembly (fixed on the rear panel—see page 7.18-4 Detail 8).

c. Turn the instrument to stand on its left side (on Left Hand extrusion).

d. Release the four M8×110mm bolts, washers and nylock nuts.

e. Remove the M3×8mm pozi-countersunk screw, M3 steel nut and shakeproof washer which secures the solder tag terminals of four ground wires. Fold back the wire which is fitted to the rear panel assembly.

f. Remove the Mains (Line) Transformer assembly.

3.5.21 LINE TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.20, referring to Page 7.15.1 for re-assembly of items to the M8 transformer bolts.

3.5.22 HF TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-4 Detail 6)

a. Remove four M3×8mm pozi-pan screws (Page. 7.18-4 Detail 6).

b. Disconnect connectors at the following points:

J2—High Voltage Assembly;
J5—Power Amplifier Assembly.

c. Remove the HV transformer assembly.

3.5.23 HF TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.22 referring to Page 7.15-2 for assembly of items to the M4 transformer bolts.

3.5.24 LF TRANSFORMER ASSEMBLY—REMOVAL
(Page 7.18-5 Detail 10)

a. Remove High Voltage assembly 3.5.18 and the Heatsinks 3.5.16.

b. Disconnect connector J2 and J5 from the Power Amplifier and High Voltage assembly.

c. Turn the instrument to stand on its right hand side (on R.H. extrusion).

d. Remove the HV transformer assembly.

3.5.25 LF TRANSFORMER ASSEMBLY—FITTING

Reverse procedure of para. 3.5.24 and refer to Page 7.15-2 for assembly of items to the M4 transformer bolts.

3.5.26 TERMINAL PCB ASSEMBLY
(Page 7.17-3)

Access:
Front panel (para 3.4.5)

a. Remove the four M3×6mm pozi-pan screws (7.18-4 Detail 8)

b. The terminal board can be tipped down to facilitate component access.

3.5.27 TERMINAL PCB ASSEMBLY—FITTING

Reverse the procedure of para 3.5.26.

3.5.28 REAR PANEL ASSEMBLY—REMOVAL
(Page 7.18-6)

WARNING.
DO NOT REMOVE THE REAR PANEL ASSEMBLY WHEN TOP AND BOTTOM COVERS AND GROUND/GUARD ASSEMBLIES ARE REMOVED.

Note:
This procedure provides access to rear panel-mounted components by releasing the Rear Panel assembly and moving it away from the chassis to the extent allowed by internal wiring connections.

Perform the following operations with Top and Bottom Covers and Ground/Guard assemblies fitted, or with AT LEAST the Top OR Bottom Ground Sheet assembly fitted.

a. Remove the six screws of the two rear spacers 7.18-4 Detail 7.

b. Remove the two rear spaces.

c. Remove the four screws of the filter grill.

d. Remove the filter grille and filter.

e. Remove the Pozi-pan screw revealed by the removal of the filter and grill.

f. Remove the four rear panel screws (Page 7.18-4 Detail 6).

g. Looking at the rear, locate the upper right hand screw, securing the extractor fan. Above this screw, locate an M3×6mm Pozi-pan screw. Removal of the latter allows the rear panel to be detached (see cut-away sketch of Rear Panel in Detail 6 of page 7.18-4).

CAUTION—Do not stress the wires.

h. Gently pull the Rear Panel assembly away from the chassis to the extent allowed by the wiring.

3.5.29 REAR PANEL ASSEMBLY—FITTING

a. Press the Rear Panel assembly to the chassis while ensuring that:

1. The wires lay in the cut-out in the moulded internal chassis;
2. The ribbon cables fit in the recess in the moulded internal chassis;
3. All other wires are free and not trapped by the rear panel assembly.

b. Fit screws, filter, filter grille and rear spacers, reversing the procedure of para. 3.5.28.

SECTION 4

TECHNICAL DESCRIPTION

4.1 PRINCIPLES OF OPERATION

SIMPLIFIED BLOCK DIAGRAM

Fig. 4.1.1. illustrates the general functions and signal flow within the 4200.

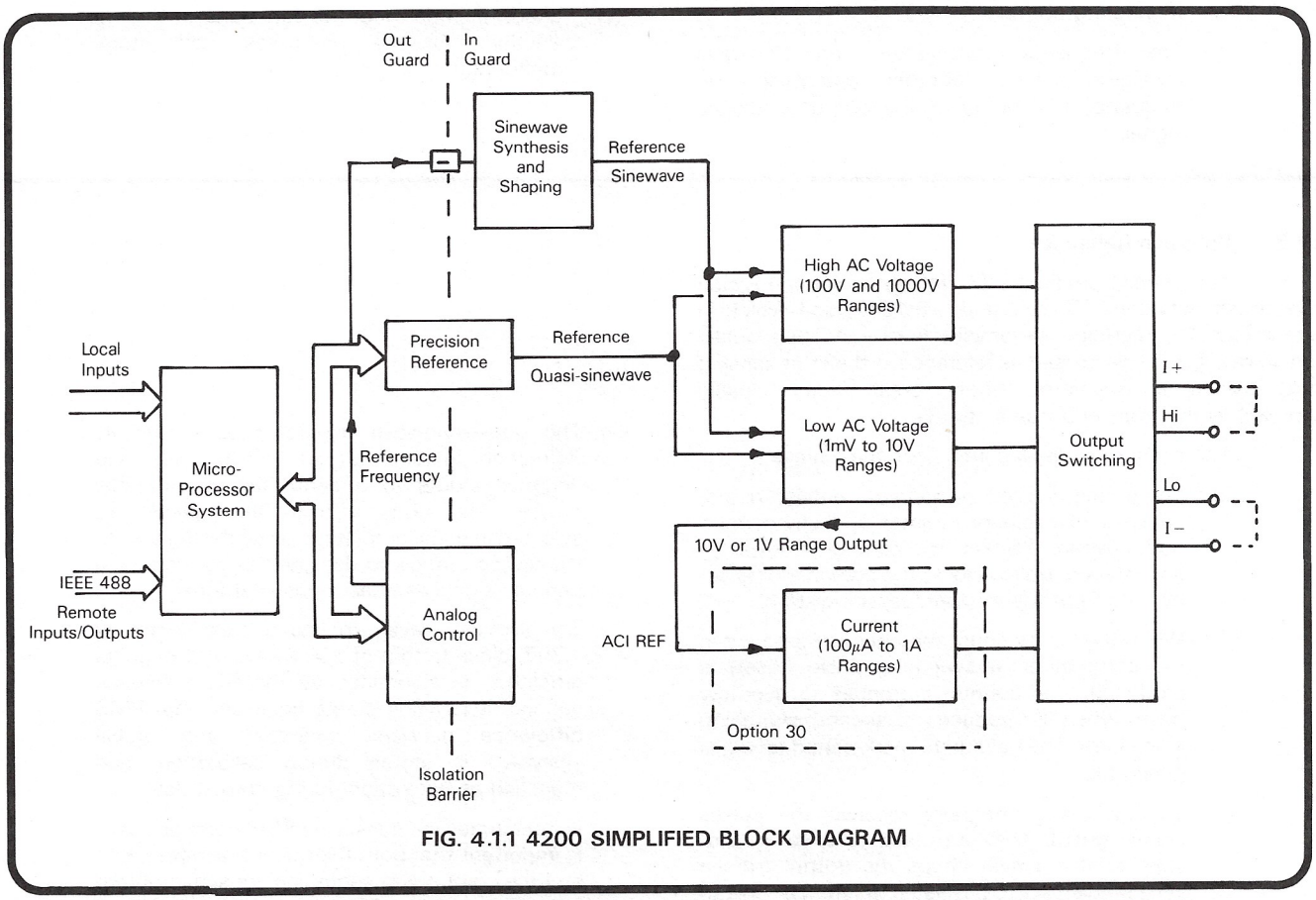


FIG. 4.1.1 4200 SIMPLIFIED BLOCK DIAGRAM

The 4200 AC calibrator is an accurate sinewave source, whose output frequency and amplitude are determined by user-inputs (within the specifications detailed in the User's Handbook).

Internally, the calibrator output frequency is synthesized using a crystal-controlled oscillator as a frequency reference. For amplitude control, an adjustable precision reference is derived from pre-conditioned zener diodes.

FUNCTIONAL BLOCK DIAGRAM

FIG. 4.1.2 (overleaf) breaks the main functional divisions into smaller blocks. It can be thrown clear of the handbook to provide a functional overview; it is also an index to other subsections of Section 4.

4.1.1 Inputs

The microprocessor accepts inputs from two main sources:

(i) The front panel keyboard provides local control inputs.

(ii) The IEEE 488 bus system provides remote control inputs.

4.1.2 Digital Outputs

The microprocessor system outputs digital information to five main areas:

(i) The front panel displays provide local monitoring outputs.

(ii) The IEEE 488 bus system provides remote monitoring outputs.

(iii) The frequency synthesizer and sinewave oscillator, which together determine the frequency and purity of the output sinewave signal.

(iv) The precision reference generator produces a reference quasi-sinewave to determine the amplitude of the output signal.

(v) Various decoders control functions and range selection, internal processes and status monitoring.

4.1.3 Precision Reference

The circuits produce a DC reference voltage which can be set between +0.126V and +2.794V, and which in turn is used to determine the amplitude of a stepped 'quasi-sinewave' signal. This is used as reference in the error sensing loop, having a waveform whose crest factor closely approaches that that of a true sinewave.

The circuitry is divided into three main areas:

(i) The period division comparator, outside guard, consists of a binary counter and comparator, both covering 25 bits. The counter is driven by a crystal-controlled clock; the comparator is set by data from the microprocessor system.

When the binary count matches the data set in the comparator, a switching pulse (reset) is produced. The counter continues to overflow point when it produces a second switching pulse (set). Thus accurate mark-period timing is generated.

(ii) The switching integrator receives the pulses across guard. They are used to drive a solid-state switch which chops the output from a very stable 20V DC Master Reference. This in turn produces a square wave which is very accurately defined both in mark-period ratio and amplitude.

This resultant square wave is integrated by an active low-pass filter with high rejection at the chopping frequency, to produce the DC Reference.

(iii) The quasi-sinewave generator uses the DC Reference voltage to set the positive and negative inputs to a center-tapped potential divider. The outputs from the divider are selected in equal time-steps by digital logic, with the division ratios so designed as to produce a periodic signal of quasi-sinusoidal form.

The signal's waveform has a crest factor of 1.397, close to that of a sinewave. Although its amplitude is adjustable by the DC Reference voltage, it remains stable once set. The RMS difference between sinewave and quasi-sinewave is stored during calibration, and reapplied as correction during normal use.

For accurate sine/quasi-sine RMS comparison, it is important that both the quasi-sinewave steps and the comparator sequence are synchronized to zero-crossing points in the sensed output sinewave. This is ensured by including the divide-by-ten logic of the quasi-sinewave generator as part of the range-divider chain for the frequency synthesizer. The quasi-sinewave frequency is also fed to the comparator, to synchronize a ten-step sequence which controls the RMS comparison process.

4.1.4 Analog Conrol

The analog circuitry is controlled by data held in a 48-bit in-guard latch. The microprocessor regularly updates the latch contents, using the serial link to pass the data (through opto-isolators) across the isolation barrier. Certain analog status signals are returned to microprocessor, also using the serial link.

4.1.5 Sinewave Synthesis and Shaping

The frequency synthesizer and quadrature oscillator together generate a reference sinewave of stable amplitude and high purity.

4.1.5.1 Frequency Synthesis

The user-demanded frequency is related to frequency range selection and expressed as a binary number 'n' by the microprocessor. It is passed into guard together with binary-coded frequency-range data, to control the frequency of the synthesizer.

The master crystal-controlled clock, at 4.096MHz, clocks the binary counter outputs in the reference divider. The counter outputs a 16kHz frequency reference signal to the synthesizer, where it is divided by two to 8kHz.

In the synthesizer, binary subdivisions of 'n' switch the capacitors of a voltage-controlled oscillator, adjusting its relaxation time-constant so as to cover five possible frequency bands within each frequency range. The VCO output frequency is divided by 'n', then compared in phase with the 8kHz reference. The integrated output from the phase comparator controls the charge and discharge current of the capacitors in the VCO. Thus the VCO frequency is adjusted to $n \times 8$kHz.

The frequency range data is decoded and used to define division ratios in a series of frequency dividers, which act on the output from the VCO. The result is the user-selected frequency, to an accuracy of 100ppm.

4.1.5 Sinewave Shaping

The binary number 'n' and the decoded frequency range data switch the circuit constants of the quadrature oscillator, to tune it approximately to the user-selected frequency. The oscillator and synthesizer frequencies are input to a second phase comparator, whose output pulls the oscillator frequency to that of the synthesizer.

The quadrature oscillator feedback is conditioned to ensure that 360° loop phaseshift occurs only at a specific amplitude; at the synthesized frequency.

The oscillator output is fed as reference sinewave to the VCA.

4.1.6 Low AC Voltage Output

4.1.6.1 Voltage-Controlled Amplifiers

The output from the quadrature oscillator is applied to two cascaded voltage-controlled amplifiers. The gain of the second of these (the 1V buffer) is adjusted in coarse steps; the gain of the first being adjusted in response to the error between the sensed and scaled output amplitude and that of the quasi-sinewave reference.

The settling curve of the 7-pole filter in the precision reference divider is imposed on the 1V buffer slew rate, by using the filter's DC reference output as control for the coarse gain. This signal is changed into a ten bit number by an analog-to-digital converter, whose digital output adjusts the input resistance of the 1V buffer in steps of 1000ppm of Full Scale. To compensate for the effect of this control on the gain of the error loop, the same 10-bit word is used to scale the error signal applied to the first VCA.

4.1.6.2 Low Voltage Outputs

On the 1V range, the output from the 1V buffer is passed to the I+ and I+ terminals directly.

For the 10V range, the 10V amplifier (on the Power Amplifier assembly) is included in the output path to the I+ and I− teminals.

For the millivolt ranges, the 1V buffer output signal is reduced by switched, passive attenuators before being output via the Hi and Lo terminals.

4.1.6.3 Low Voltage Sensing

On the 1V range, the input from the Hi and Lo (sense) terminals is applied to the non-inverting input of the 1V/10V sense amplifier, which acts as a voltage follower.

For the 10V range, the sense amplifier is configured as a divide-by-ten inverter.

For the millivolt ranges, there is no remote sensing. To complete the sense feedback, the 1V buffer output is input directly into the sense amplifier, which is a configured as for the 1V range.

4.1.6.4 Sine/Quasi-Sine RMS Comparator

In a strict sense, this circuit does not compare RMS values directly. Instead, it compares the magnitudes of the mean-squares of its two inputs, but if these are equal, then the RMS values are equal.

A cycling sequence is continuously imposed, each cycle with a duration of ten quasi-sinewave periods, whereby during the first cycle:

(i) the quasi-sinewave input is first squared and integrated as a DC analog reference;

(ii) the DC reference is memorized in a sample-and-hold circuit;

(iii) the sensed sinewave is squared, the DC reference value in (ii) being subtracted from the squared value;

(iv) the DC analog result is memorized in a second sample-and-hold circuit, and output as the AC error signal.

On subsequent cycles, the DC reference is also subtracted from the squared quasi-sinewave, so that both DC reference and AC error signals converge to steady states as the 4200 output reaches the demanded voltage.

The AC error signal is passed through the error scaling circuit to control the VCA.

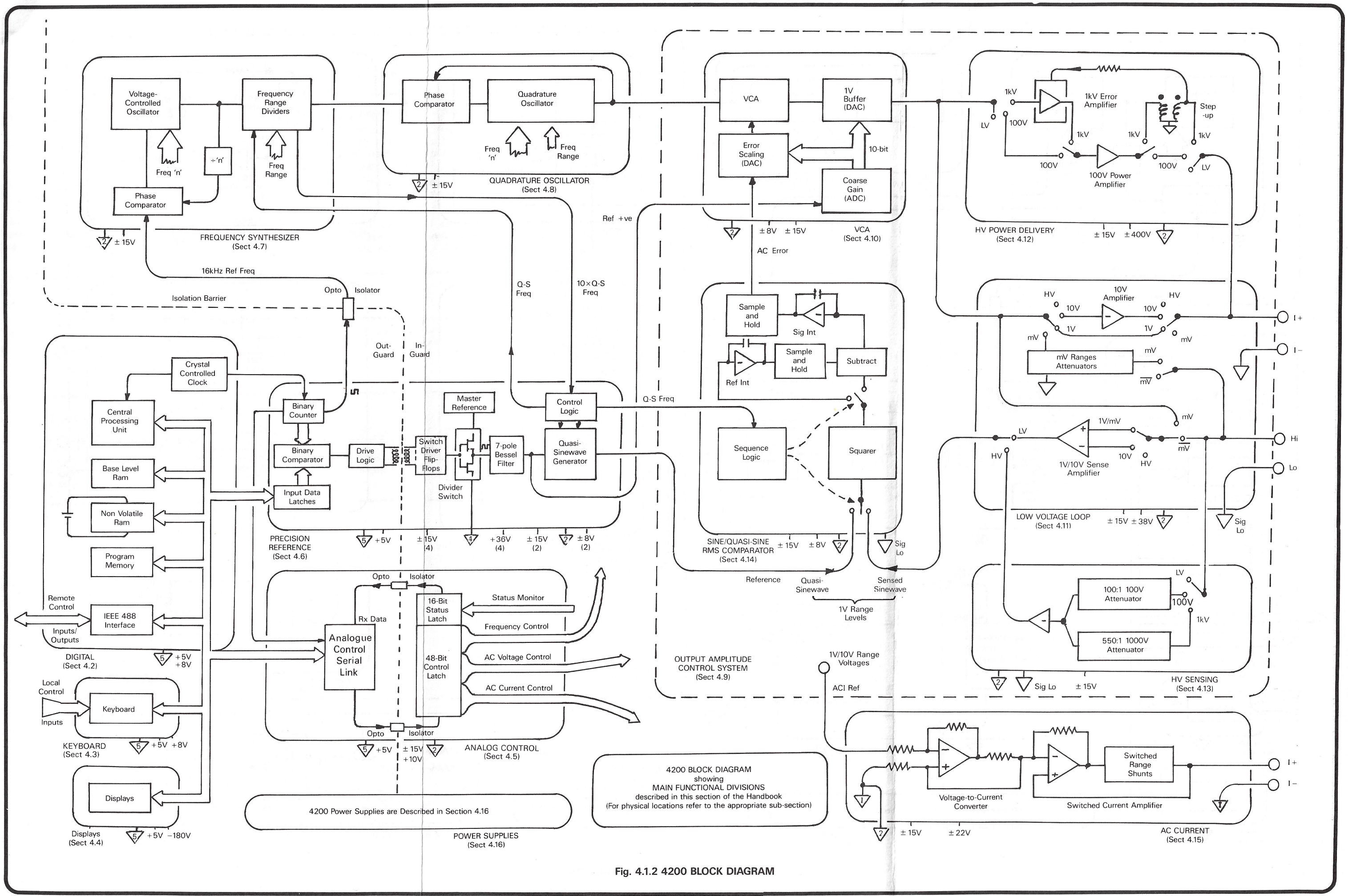


Fig. 4.1.2 4200 BLOCK DIAGRAM

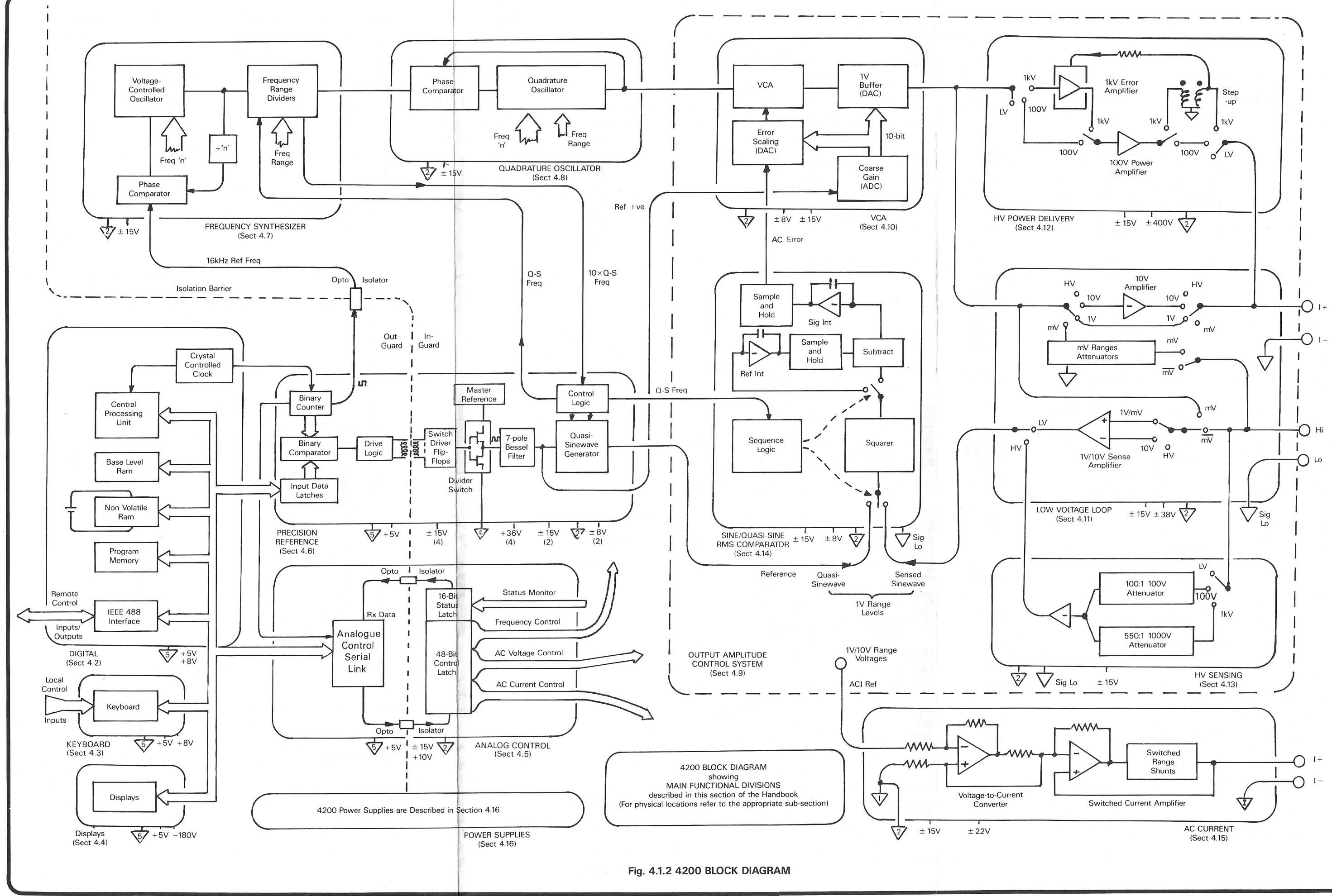


Fig. 4.1.2 4200 BLOCK DIAGRAM

4.1.7 High AC Voltage Loop

The high voltage loop uses much of the low voltage circuitry; the only differences being in the power amplification to the range voltages, and the attenuation of the sensed output down to 1V range levels.

4.1.7.1 High Voltage Outputs

On the 100V range, the 100V amplifier (on the Power Amplifier assembly) is included in the output path from the 1V buffer to the I+ and I− terminals.

On the 1000V range, the output from the 100V amplifier is transformed up by 6:1 before being passed to the I+ and I− terminals. An error amplifier is inserted in the input to the 100V amplifier to receive the feedback from the transformers; the HF transformer is selected as frequency is increased above 3kHz, and the other (LF) as frequency is reduced below 3.3kHz.

4.1.7.2 High Voltage Sensing

A separate inverting sense amplifier is used for the 100V and 1000V ranges. The basic amplifier is common to both, but each range has its own input attenuator and feedback ratio.

On the 100V range, the amplifier reduces the sensed sinewave by a ratio of 100:1, but on the 1000V range this ratio is 550:1.

For the 1000V range only, software scales the reference divider digital input to set the quasi-sinewave RMS value to the equivalent of 1100V Full Scale.

4.1.8 Current Output (Option 20)

For Current outputs either the 10V (for the 1mA, 10mA and 100mA ranges) or 1V (for the 100μA and 1A ranges) range circuitry is activated to generate the ACI reference signal. This is switched to drive a voltage-to-current converter, followed by current amplifier.

The various ranges are selected by digital control signals from the microprocessor system. Shunts in the current amplifier are switched into the output circuit to scale the current.

4.1.9 'AUTOCAL'

Although the instrument's circuitry utilizes precision components in all critical locations; frequency roll-off, offset and gain errors remain (in analog terms) uncorrected. At calibration these errors are measured and stored digitally in non-volatile memory.

In subsequent use, characteristic equations are applied to the stored errors to generate software corrections, which are then used to modify the reference divider ratios and so compensate for the analog errors.

4.2 DIGITAL

The circuits described in this section perform the following functions:

(1) Central processing, with supporting memory, for management of instrument operation.

(2) Storage of calibration constants in non-volatile memory.

(3) Generation of Master clocks, with clock-waveform shaping.

(4) Address decoding to generate control signals.

(5) Controlled power-up and power-down of digital circuits.

(6) Servicing IRQs from asynchronous sources.

(7) Interfacing the 4200 to the IEEE 488 bus.

The functions are performed by circuits located mainly on the Digital PCB Assembly (400534). Master Clock generation, synchronization and division is carried out by circuits on the Analog Interface PCB Assembly (400570).

Fig. 4.2.1 shows the arrangement and main inter-connections of the central digital circuits.

4.2.1 General

The 4200 is managed by a 6802-series microprocessor system, under the control of an operating program held in 24k bytes of EPROM. All front and rear panel controls provide direct inputs to the sysem, except for the Power ON/OFF switch and Safety Reset Key. The System ensures that the processor reverts to a safe state on power-up and power-down.

2k bytes of random-access memory (RAM) are used for work space and stack. A further 2k bytes of CMOS RAM act as a non-volatile memory to hold calibration constants, powered by a back-up Lithium battery when the instrument is turned off.

4.2.1.1 Synchronous Operation

The operating program manipulates the internal circuitry by activating control signals. These result from providing peripheral decoders with specific address combinations. The program is run at 680kHz cycling frequency, originally derived from a 4.096MHz master crystal oscillator.

4.2.1.2 Asynchronous Operation

Any Key operation (other than Safety Reset), or one of two internal conditions, will initiate an asynchronous interrupt (IRQ) which suspends the CPU's current task. The CPU absorbs the new instructions, rearranges its schedule to conform to the demanded new configuration, then continues with the interrupted task until it is completed. It next returns to the initial operation of the amended task schedule and proceeds synchronously.

Three main sources of interrupt are used:

Remote Command via the Digital Interface

Keyboard Command

Real-time Clock Pulses (8ms intervals)

The CPU identifies the source by polling the data bus each time it receives an IRQ interrupt.

4.2.1.3 Output Generation

From user inputs of output value, frequency, error and calibration constants, the CPU computes a binary value to a resolution of 25 bits. This is used to adjust the mark/period ratio of the Reference Divider switch which ultimately controls the Working Reference Voltage for the output analogue circuitry.

4.2.1.4 Display Refresh

The gas discharge display is continuously refreshed by cycling through character data stored in a separate display-image RAM. To alter the display the processor merely alters the contents of the RAM.

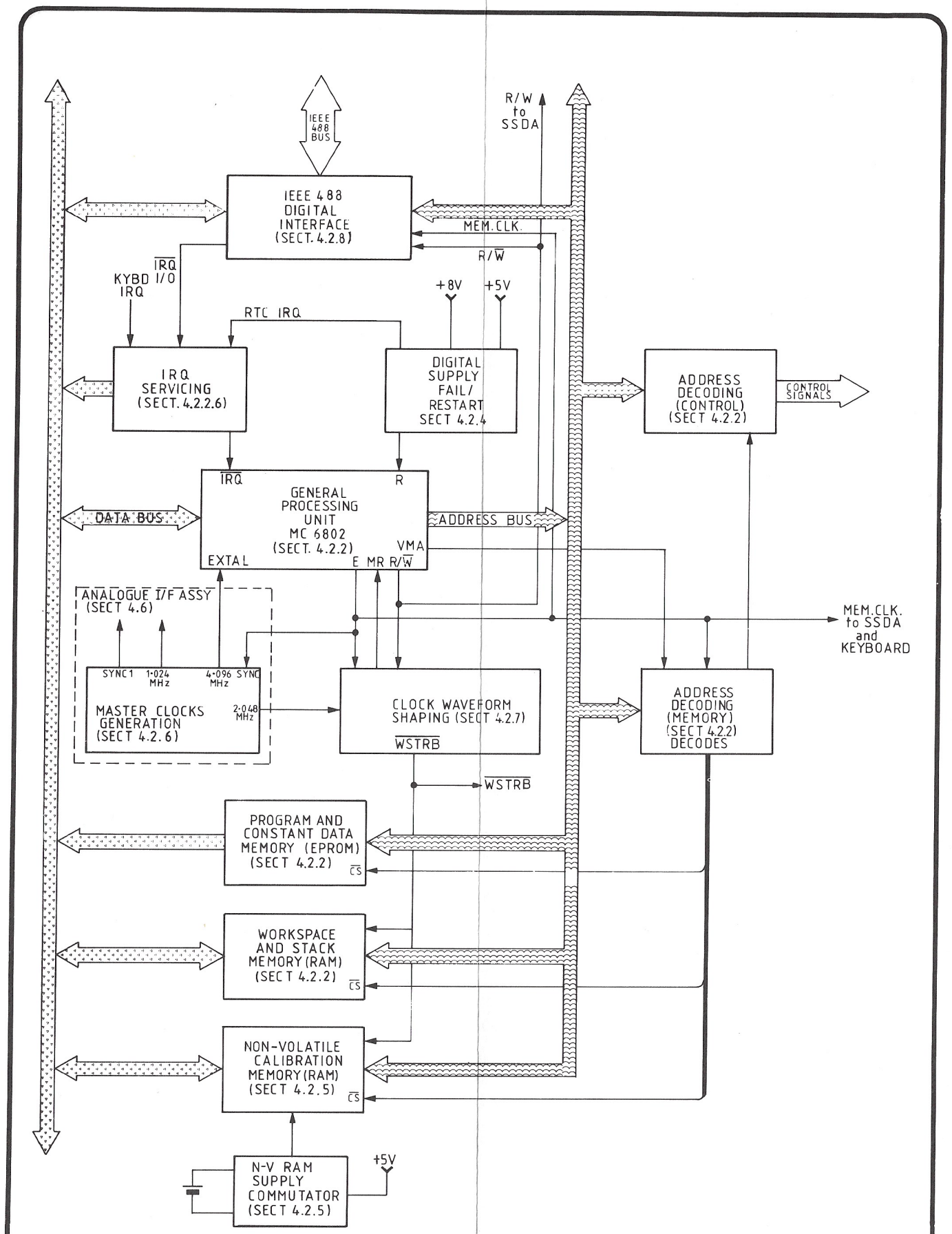


FIG. 4.2.1 4200 DIGITAL FUNCTION BLOCK DIAGRAM

4.2.2 Central Processor and Memory

(Circuit Diagram 430534 Pages 7.2-2 and 7.2-3)

A 6802 microprocessor, (M34), together with its memory, controls communication throughout the whole instrument.

4.2.2.1 Memory

The memory can be split into five main areas:

(1) Program Memory (M19, 20, and 21)	defines and controls the operational functions of the whole instrument system.
(2) Constant Data Memory (held in EPROM with the Program Memory)	e.g. Instrument specification for use in 'Spec' mode, key mapping tables and other fixed factors.
(3) Non-Volatile Calibration Memory (M23)	stores all the calibration constants, determined during the 'Auto-cal' cycle, which are used for each output value.
(4) Volatile Memory (M22)	used for volatile data storage, e.g. display images, computational stores, present output value.
(5) Operating Memory (M22)	used for scratch pad operations and storage.

The 6802 microprocessor internal RAM is not used.

Separate memory is used for special purposes, such as the Display Image RAM (M16) which is synchronously loaded but asynchronously read; the storage areas in the IEEE 488 GPIA (M29) and the Keyboard Interface (M6 on Front Assembly); and the Memory Address decoder PROM (M3). These are described in later sections.

4.2.2.2 Central Processing Unit

(Circuit Diagram 430534 Page 7.2-2)

The MC6802 (M34) is a monolithic 8-bit microprocessor, with interrupt and clock-stretching facilities. It is driven by a single phase 4.096MHz square wave generated by the Master Clock X1 in the Analog Interface Assembly. (This clock synchronizes the reference divider switch with the processor cycle).

4.2.2.3 Address and Data Lines

Address lines $A_{15\text{-}11}$ are decoded as chip-select signals for the RAM/ROM circuit, and lines $A_{13\text{-}\emptyset}$ are connected to the instrument address bus. Data lines $D_{7\text{-}\emptyset}$ are linked via programming plug JL1 to the instrument data bus.

4.2.2.4 E, MR and MEMCLK

The 4.096MHz clock input at M34-39 (EXTAL) is divided by four and used as output at M34-37(E). Although the natural frequency of E is 1.024MHz, the action of the waveform shaping input to MR reduces it to approx. 680kHz as MEMCLK for the Front and Analog-Interface assemblies.

4.2.2.5 $\overline{\text{NMI}}$

The internal switch S1 provides a non-maskable hardware interrupt which has two functions.

(1) With the external CALIBRATION switch set to RUN, $\overline{\text{NMI}}$ initializes the processor system.

(2) With the CALIBRATION switch set to ENABLE, $\overline{\text{NMI}}$ clears the non-volatile calibration memory (M23) before initializing the processor system.

4.2.2.6 $\overline{\text{IRQ}}$

Any one of three asynchronous Interrupt Request signals are able to activate the maskable $\overline{\text{IRQ}}$ input at M34-4:

(1) RTC IRQ is a real-time clock which occurs every 8ms to provide timing information for the processor's monitoring facility.

(2) KYBD IRQ occurs each time a front panel key is depressed. (Not Safety Reset).

(3) $\overline{\text{IRQ}}$ IO occurs when the IEEE 488 Interface has a transaction to communicate to the processor.

D1, D2 and Q1 constitute a DTL OR-gate to isolate the IRQ inputs from each other. On receipt of Logic-Ø on pin 4, M34 stores its register contents in stack RAM, and vectors to IRQ service addresses FFF8 and FFF9, saving the current processor environment.

The IRQ Service Routine addresses M51 and M52, generating logic-Ø at M52-9 which enables the tristate buffers M36 and M37 at M36-1 and 15, M37-15. This sets IRQ data bits D5, D6 and D7 on the data bus so that the processor can identify the source of the IRQ and select the appropriate sub-routine to service the interrupt request.

The IRQ inputs are released as part of the service sub-routine, and after its completion, the processor recovers its environment from stack RAM and proceeds with the interrupted operation.

4.2.2.7 Software Interrupt

The 6802 will also recognise Opcode 3F on the data bus as an interrupt request ('Implied' addressing mode'). In the 4200 this code is hard-wired via R9, R10 and AN3 onto the data bus so that if the CPU tries to access a non-available address, the floating bus will be pulled to 3F, initiating the software interrupt. The CPU vectors to FFFA and FFFB, whose contents cause the 6802 to re-initialise the whole system.

4.2.2.8 Read-write line R/$\overline{\text{W}}$

The processor sets the R/$\overline{\text{W}}$ line to logic-1 when it is in Read state, and logic-Ø when it has data to write into the addressed device. The R/$\overline{\text{W}}$ signal is passed only to the SSDA on the Analogue Interface assembly, and to the IEEE 488 GPIA (M29). All other devices which require read-write control, operate from RDSTRB and WRTSTRB signals generated from R/$\overline{\text{W}}$ by M49/50.

4.2.3 Software Overview

The software management organisation is shown in Figure 4.3.2. The machine cycle, which progresses through the task schedule shown, is modified by the requirements of real-time-conscious activities and by those dedicated to remote commands. Real time and remote command interrupts suspend the current activity of the processor in order to service the immediate task requirement; the suspended task is then resumed.

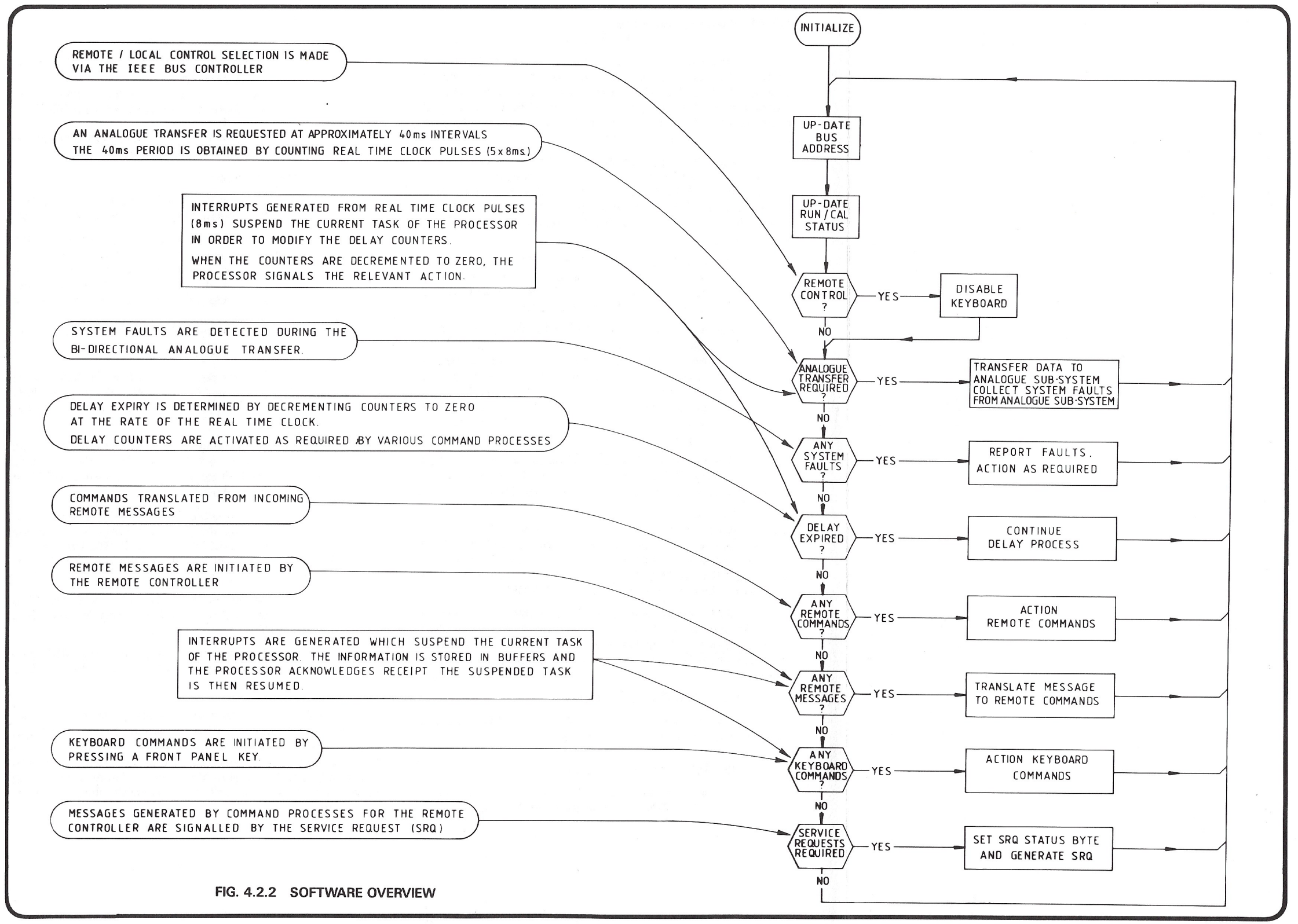


FIG. 4.2.2 SOFTWARE OVERVIEW

4.2.4 Digital Supply Fail/Restart Circuitry

Power-up, restart and shut-down of the digital circuitry are performed in a controlled sequence to safeguard against hardware failures or a software crash. A continuous surveillance of the software management is performed by the safety monitor (Watchdog — refer to Section 4.5). This will shut-down the instrument in the event of a failure in either the digital control circuits or in software management.

4.2.4.1 Power-up Sequence

(Circuit Diagram 430534 Page 7.2-2)

Power-on is first sensed by the Supply Fail Detector circuit. This draws its supplies from the +8V DC unregulated supply, which is the first of the power supplies to rise to a working level. The comparator circuit of M28 has a nominal threshold of +7.1V DC, above which a good working level of the +5V DC supply is assured.

As the +8V supply rises, below +7V, M28-2 follows until Zener D6 avalanches, when it is held at +2.45V. At this level M28-3 voltage is less than 1V, so M28-1 remains at 0V holding M8-5 'D' input at logic-Ø and M7-3 at logic-1. Thus M8 and M9 are held in reset, initiating and maintaining the following state:

(1) M8-2 ($\overline{Q}$) at logic-1, PWR ON RST active. Fed to the front panel assembly, this logic-1 level holds keyboard encoder M6 in Reset and disables the LED cathode driver decoder M4.

(2) M6-4 at logic-Ø, $\overline{\text{PWR ON RST}}$ active. This logic-Ø level holds the microprocessor M34 in Reset state. Its VMA output at M34-5 is held at logic-Ø disabling address decoder M3, setting all M3 address outputs to logic-1. This combination gives logic-1 at M5-13, but M6-2 at logic-Ø gives logic-1 at M5-11 and subsequently logic-1 at M7-2.

The logic-Ø of $\overline{\text{PWR ON RST}}$ also holds the IEEE 488 GPIA M29 (page 7.2-4) in Reset. It is also fed to the Analog Interface assembly where it holds the SSDA M44 in Reset.

When the +8V supply rises above about +7.1V, M28-3 voltage rises above the +2.45V on M28-2, so M28-1 rises to place a logic-1 both on M8-5 (D input) and M7-1. M7-3 falls to logic-Ø, removing the resets from 14-bit counter M9 and restart flip-flop M8. So M8 is enabled to receive its clock from M9, which itself is clocked from 2.048MHz.

At full count, 8ms after M9 is enabled, M9-3 clocks M8. As M8 'D' input is already at logic-1, this is clocked through to M8-1 (Q), and logic-Ø to M8-2 (Q). PWR ON RST and $\overline{\text{PWR ON RST}}$ change to their inactive states, and start-up proceeds:

(1) PWR ON RST at logic-Ø.:

Enables keyboard encoder M6 and LED cathode driver decoder M4 on the Front assembly.

(2) $\overline{\text{PWR ON RST}}$ at logic-1:

a. Removes reset from CPU M34, allowing software initialization to commence, and enables IEEE bus controller M29 on the Digital assembly.
(Part of the instrument initialization procedure is a software reset for M29).

b. Removes reset from the SSDA M44 on the Analog Interface assembly.

(3) M8-1 to logic-1:

a. Provides an enabling input to M10-1 (See Non-Volatile RAM Supplies Section 4.2.5).

b. Triggers monostable M53-4. This monostable has a relaxation period of 470ms; during which time it holds the $\overline{\text{FP RST}}$ output at logic-Ø, allowing the watchdog circuits to reset on the Reference Divider.
(See Safety Monitor Section 4.5).

c. Enables RTC IRQ via M7-13.

Address decoder M51-5 is normally held at logic-1, so M7-11 and M8-10 at logic-Ø allow M9-3 clock to affect the RTC IRQ output at M8-13.

For so long as the +8V supply holds up above +7.1V, M9 continues cycling through its full count, clocking M8-11 at 8ms intervals.

To terminate an RTC IRQ service sub-routine, the CPU addresses M51, pulsing M51-5 (M7-12) to logic-Ø (RTC RST). M7-11 is pulsed to logic-1, resetting M8-13 (RTC IRQ) to logic-Ø.

At the next full count of M9; M8-13 is clocked to logic-1, initiating the next RTC IRQ.

The actions of M9, M8 and M51 thus generate a 'Real-Time Clock IRQ' at 8ms intervals.

Pulses from M9-3 also regularly clock the binary state of M8-5 throught to M8-1, monitoring the supply status. When running normally, M8-5 and M8-1 are both logic-1. If the supply fails, M8-5 reverts to logic-Ø, but a fast reset is also provided by M7-1 logic-Ø to M8-4 logic-1, rather than waiting for the next clock pulse. M7-3 also resets the 8ms counter to zero count at M9-11.

4.2.4.2 CPU Re-start

(Circuit Diagram 430534 page 7.2-2)

Memory addressing by the CPU is monitored by the NAND logic of M4, M5 (four elements) and M7-3. In the correct addressing sequence there are two basic conditions:

(1) CPU VMA = Logic-Ø
M3-D0 to D7 = Logic-1

(2) Valid memory address:
CPU VMA = Logic-1
CPU E = Logic-1
M3-D0 to D7 = One address line logic-Ø

Conditions (1) and (2) both result in a logic-Ø from M7-3, allowing clock M9 and flip-flop M8 to function normally. The possibility of a glitch occurring at the change-over between conditions (1) and (2) is gated from the control line by switching at M5-5. Incorrect addressing sequence in the CPU would be shown by:

CPU VMA = Logic-1 } The CPU indicates that it has
CPU E = Logic-1 } selected a valid external address.
M3-D0 to D7 = Logic-1 No address is selected.

This situation is most likely with a software failure. The logic control path through M4, M5 now gives a logic-Ø at M7-2 and thus a logic-1 at M7-3 which:

(1) Resets counter M9 to zero;

(2) Forces M8-1 to Logic-Ø. This forces RTC RST at M7-11 and removes an enable from M10-1. (See Non-volatile RAM supplies Section 4.2.5).

(3) Forces M8-2 to logic-1. This change:
a. Resets the CPU by M34-40 to logic-Ø. VMA is forced to logic-Ø which in its turn removes the reset from M9-11 and M8-4 via M6-2 (at logic-Ø), and the M4-M5 control path.
b. Makes PWR ON RST and $\overline{\text{PWR ON RST}}$ signals active, thus resetting the other software-controlled areas.

After 8ms from CPU reset, flip-flop M8-3 is triggered from clock M9. M8-1 and M8-2 change state and the start-up sequence proceeds.

4.2.5 Non-volatile RAM Supply Commutation

4.2.5.1 Non-volatile RAM Inhibit (NV INHIBIT)

(Circuit Diagram 430534 page 7.2-2)

Chip-select to the non-volatile memory M23 is inhibited during power-up, re-start and power-down operations. Memory access to the non-volatile RAM is enabled during normal running by the chip-select input $\overline{\text{NV INHIBIT}}$ being held at logic-1. The NAND logic gates M10, used to control the inhibit, remain powered from the RAM standby supply after power-down.

Conditions for normal running are as follows:

(1) Supply fail detector circuit provides a logic-1 (supplies valid) output to opto-coupler M11. This causes the coupled transistor of M11 to conduct and hold M10-2 at logic-1.

(2) M10-8 is held at logic-1 (to +5V via R6).

(3) M10-1 is held at logic-1 by flip-flop M8-1.

The above conditions ensure a logic-1 output from M10-10 ($\overline{\text{NV INHIBIT}}$ not active).

During power-up, $\overline{\text{NV INHIBIT}}$ is held active until the power supplies have settled and the CPU has gained control of memory:

The input to M10-8 is delayed on the +5V supply by the time-constant C8, R6. Also, the input to M10-1 is held at logic-Ø by flip-flop M8-1 until the CPU reset is removed.

At power-down, or in the event of a supply failure, the $\overline{\text{NV INHIBIT}}$ becomes active before 5V supply fails:

The first indication of supply failure is made by supply fail detector M28 output going to logic-Ø. This cuts off the opto-coupler M11 which takes M10-2 to logic-Ø. M10-8 is held at logic-1 by the +5V supply, thus M10-9 is taken to logic-1 and M10-10 to logic-Ø ($\overline{\text{NV INHIBIT}}$ active).

In the event of a CPU reset, the $\overline{\text{NV INHIBIT}}$ is made active for the period of reset by the switching action of M8-1 and M10-9.

4.2.5.2 Supply Commutator

(Circuit Diagram 430534 page 7.2-3)

This circuit provides the non-volatile RAM M23 with a battery-driven standby supply when the instrument is in the power-down condition. It ensures continuity of supply in the change-over between main and standby, and minimizes battery current leakage.

In the power-down condition, the battery powers M10 and M23, returning from battery common (TP13) via D7 and R60. The battery common is isolated from the general common 5A by transistor Q2, which is cut-off.

During power-up, M28 is powered from the +8V supply before the +5V supply voltage becomes established. As long as the +5V supply voltage is less than the battery voltage, Q3-4 is biased negatively, and Q3 is unbalanced in favour of heavy conduction through Q3-6. M28-5 is held low, so M28-7 remains at Common-5A potential, and so opto-coupler M39 is not energized.

Q2 remains cut off, maintaining isolation of the battery supply from Common-5A.

M10 and M23 remain powered from the battery.

As the +5V supply voltage increases, D7 cathode potential rises, reducing Q3-4 bias, reaching zero when its voltage is equal to the battery voltage (less than 10mV is developed across R60).

When the +5V supply voltage exceeds the battery voltage, Q3 becomes biased in favour of heavy conduction through Q3-2, pulling M28-6 low and reversing the differential input to M28. M28-7 rises to the +8V rail and energizes the opto-coupler M39, which switches Q2 on, connecting battery common to common-5A. M10 and M23 are now powered from the +5V supply and the standby battery is isolated by reverse-biased diode D7.

During power-down, Q3 compares the +5V supply against the battery, switching Q2 off via M28 and M39 when the +5V supply voltage falls below the battery voltage, and the non-volatile RAM supply commutates to standby battery. Alternatively, Q2 is switched off by failure of the +8V supply to M28 if this occurs before the +5V supply voltage falls below the battery voltage.

Eventually the +5V and +8V supplies both fall to zero, the battery provides the supply to the non-volatile RAM, and battery common is isolated from Common-5A by Q2.

4.2.6 Master Clock Generation

(Circuit Diagram 430570 page 7.3-3)
(Refer to Fig. 4.2.3 for waveforms)

The master clock generator is based on crystal oscillator XI which provides a precision 4.096MHz squarewave reference frequency output.

The primary frequency of 4.096MHz is divided by JK flip-flop stages M41, both of which are connected to toggle when clocked. The first division stage is synchronized at its reset input, M41-3, to the memory clock via flip-flop M42. This ensures correct phasing of the 2.048MHz squarewave output from M41-14.

M41-11 and M41-10 outputs provide complementary 1.024 and $\overline{1.024MHz}$ squarewaves respectively. Monostable M40, triggered at 2.048MHz from M41-15 provides the positive-going 2.048MHz synchronizing pulses, SYNC 1.

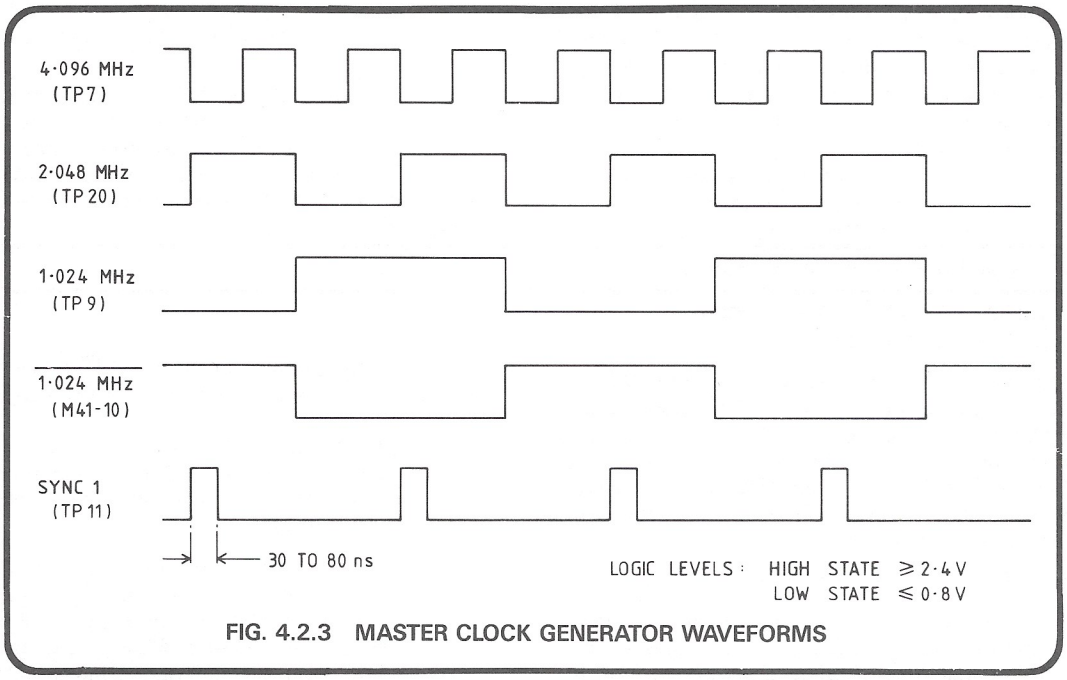


FIG. 4.2.3 MASTER CLOCK GENERATOR WAVEFORMS

4.2.7 Clock Waveform Shaping

(Circuit Diagrams 430534 page 7.2-2
and 430570 page 7.3-3)

NB As the circuit locations in Fig. 4.2.5 are clearly marked, and as there are no duplicate designators in the circuits, this description does not refer to a component's location except where necessary.

NOTE To avoid confusion, the terms 'high' and 'low' are used to replace 'logic-1' and 'logic-Ø' respectively in this description.

The crystal oscillator on the Analog Interface Assembly provides a 4.096MHz Master Clock signal (X1-8) for the whole instrument. This drives the 6802 microprocessor at M34-39 (EXTAL) so M34-38 is not connected. M41 divides 4.096MHz to generate a 2.048MHz clock for the Memory Clock Stretching Circuit (M35/M49).

The CPU (M34) divides the EXTAL input internally by 4 and outputs the result as E (Enable) at M34-37, to act as a 'Phase 2' Memory Clock for the SSDA on the Analog Interface and the keyboard controller on the Front assembly.

If M34-3 (MR—Memory Ready) were permanently held at +5V, the E signal would be 1.024MHz. But in the 4200, a 'stretching' circuit (M35/M49) doubles the Logic High (+5V) time of E by switching MR to Logic Low (0V) for part of the cycle. This is shown on Fig. 4.2.4.

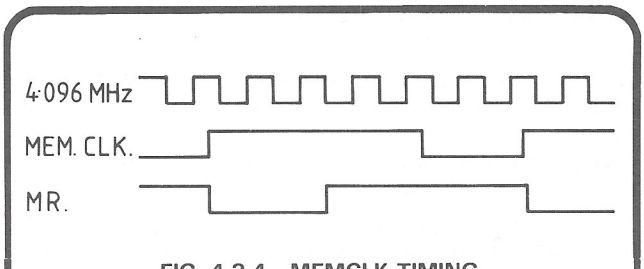


FIG. 4.2.4 MEMCLK TIMING

The frequency of E is thus reduced to approximately 680kHz, with 1μs available for access to the SSDA, Keyboard Controller, IEEE GPIA and memory.

4.2.7.1 Memory Clock Stretching Circuit
(Fig. 4.2.5)

The action of M35 and M49 is dependent upon the finite propagation time between clocks at M35-1/M35-6 and Q output at M35-15.

When M34-3 (MR) is +5V; M34-37 (E) is toggled by alternate positive-going edges of the 4.096MHz clock, with a propagation delay of approximately 80ns.

Also, the 4.096MHz signal is divided by 2 in M41, resulting in 2.048MHz signal whose negative-going edges clock M35.

M35 cascade action is controlled by the condition of the Memory Clock (E) and affected by its own propagation times.

4.2.7.2 Shaping Action
(Figs. 4.2.5 and 4.2.6)

At T1 and T2:
The 4.096MHz clock edge at T1 causes E to rise from low to high at T2. As M35-10 is also high, MR changes from high to low at T2, holding E high. M35 pin state is 4 and 10 high, 9, 12 and 16 low.

At T3 the 2.048MHz falling edge clocks M35, and M35-9 rises to high awaiting the next clock edge (not until T5). M35-10 remains high, so MR is held low and E stays high.

At T4, MR is still low, so the 4.096MHz clock has no effect on E, and E is stretched.

At T5, MR is returned to high when the logic-1 on M35-9 is clocked as a logic-Ø to M49-4. This allows the 6802 to toggle E at the next effective clock edge.

At T6 the rising edge of the 4.096MHz clock causes E to fall to low, setting up M35-4 to low, M35-12 and 16 to high. M35-9 is already high.

At T7, M35-10 is toggled to high, but as M49-5 is now low, MR remains high to allow E to be toggled at the next effective processor clock edge (not until the next T1).
Also at T7, M35-15 is clocked to low to set M35-9 ready for the next (T3) clock edge. The circuit is now set up to its initial (pre-T1) condition so the action repeats.

4.2.7.3 M41 Reset
(Fig. 4.2.5)

A remote possibility exists, that a severe disturbance could upset the synchronization of the 'E' signal with the 2.048MHz clock. To guard against this, M42 acts as a monostable to provide negative reset pulses into M41-3. Under all normal conditions, these will occur when M41 is already toggled in its reset state.

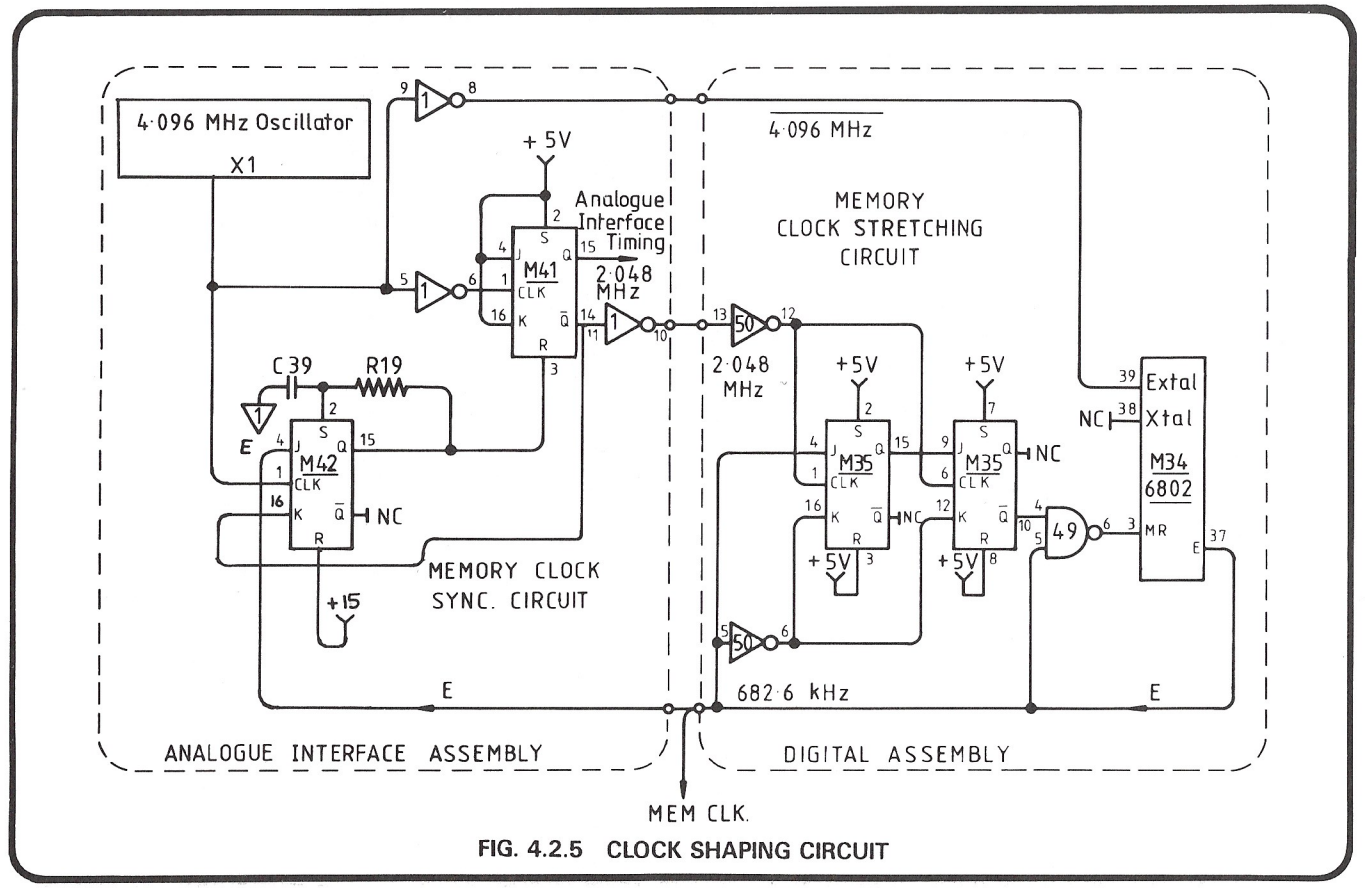


FIG. 4.2.5 CLOCK SHAPING CIRCUIT

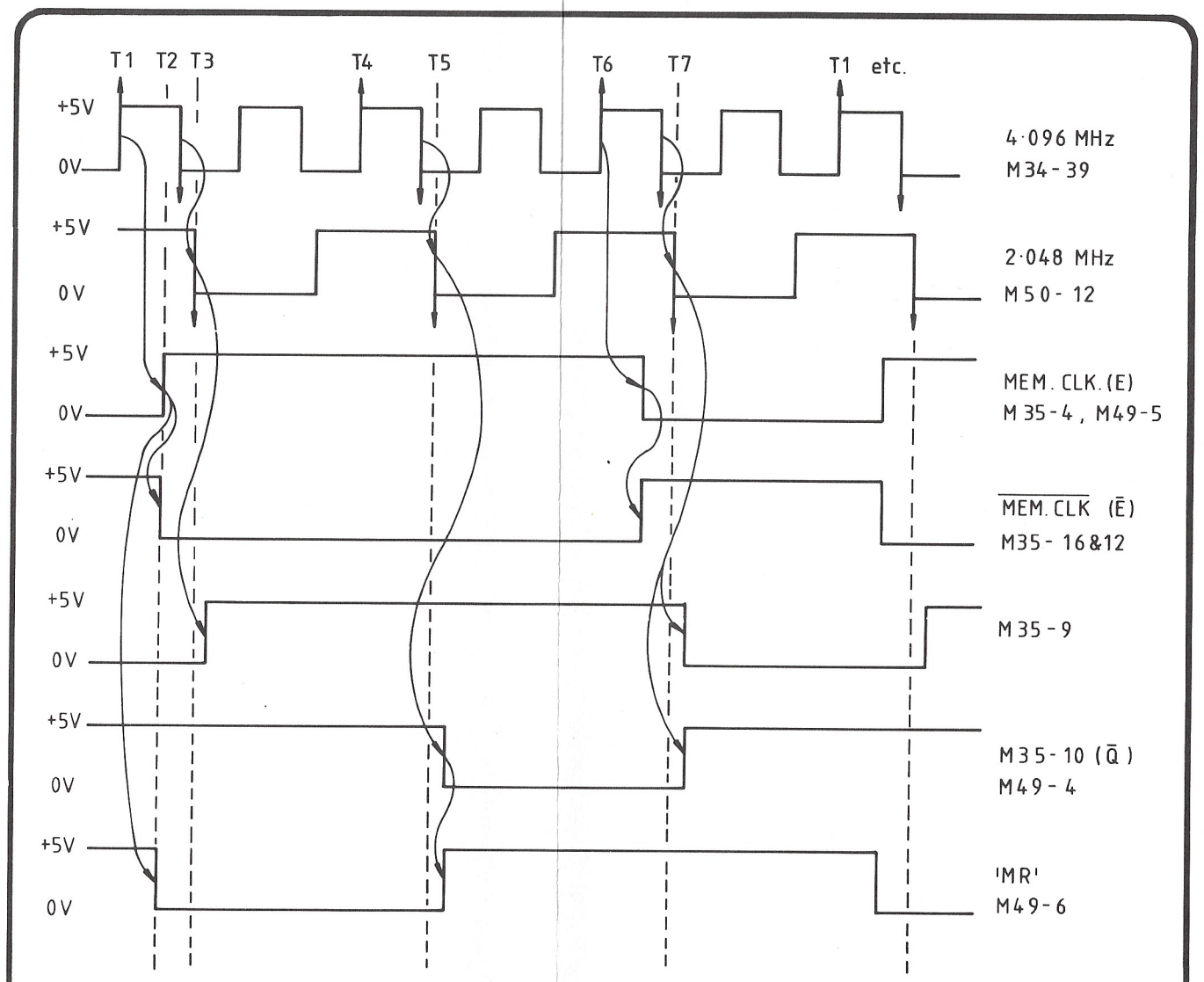


FIG. 4.2.6 CLOCK SHAPING WAVEFORMS

4.2.8 IEEE 488 Digital Interface

(Circuit Diagram 430534 Page 7.2-4)

The IEEE Interface circuitry is located on the bottom right-hand corner of the Digital PCB (viewed from the front of the instrument). M29, M40, M47 and M48 execute and decode interface functions, and transfer data (input/output).

The General Purpose Interface Adaptor (GPIA) M29, is software-driven by the 6802 CPU, as part of its normal function. M29 is addressed at C5 by $\overline{\text{XIOBBD}}$ from M51, and its internal registers are accessed by A_0, A_1 and A_2 from the address bus.

The GPIA is clocked by Memory Clock E, with read or write control direct from the processor R/$\overline{\text{W}}$ signal at M29-5, and at 4200 power-on M29 is initialized at M29-19 by the $\overline{\text{PWR ON RST}}$ signal from the Restart Generator circuit (M6-4).

Information is passed between M29 and the CPU (M34), via the data bus D_0-D_7. The address switch data is linked to D_0-D_6 by tristate buffers M47. During initialization and at subsequent intervals, the state of M29-4 (ASE) changes from +5V to 0V, enabling M47. The status of the address switches on the 4200 rear panel is transferred into M29 via M47 and the data bus for comparison with the received address.

M40 and M48 are bidirectional bus-driver arrays. The drivers for bus management lines: IFC, ATN and REN are permanently held in Receive state, and the SRQ driver in Transmit state. The EOI line driver is switched from Receive to Transmit by M29-28 (T/$\overline{\text{R}}$1) changing from 0V to +5V as required by M29. M29-27 (T/$\overline{\text{R}}$2) is normally held at 0V for reception of system data via DIO 1-8 bus lines, and set to +5V for 4200 data to be sent over the bus.

Some system controllers output excessive noise along the REN line. To avoid spurious switching of M29 between Local and Remote control states, the noise is filtered by R58 and C31.

Difficulty has been experienced with certain controllers in that NDAC can transfer data on to the bus too early. R62 and C7 slows down the transitions of NDAC to overcome this problem.

M29-40 ($\overline{\text{IRQ}}$) is used to inform the CPU when certain states occur. In particular, the $\overline{\text{IRQ IO}}$ signal is generated at each byte-transfer over the bus, whether the byte is sent or received. Additionally, $\overline{\text{IRQ IO}}$ is activated whenever certain specific commands are received, e.g: 'DAC', 'SPA', and changes between Remote and Local Status.

When the CPU receives $\overline{\text{IRQ IO}}$, it addresses M29's 'Interrupt' Status Register, then M29 identifies the reason via the instrument data bus.

For further information refer to 'Getting Aboard the 488 Bus' published by Motorola, or the appropriate device data sheets.

4.3 KEYBOARD

(Circuit Diagram 430533 Page 7.1-1)

The circuitry described in this section performs the following functions:

(1) Provides front-panel operator control of 4200 Output, Function, Range and Mode circuitry, by push-button keys. Key operation is detected internally and transferred to the CPU via the instrument data bus.

(2) Indicates the current instrument state by means of LEDs fitted in the Keys.

(3) Generates audible warning of high voltage at the Output Terminals.

In addition a rocker switch sets instrument Power ON and OFF (refer to Section 4.16) and a 'Safety Reset' Key provides a hardware reset for the safety monitor (Watchdog) circuits (refer to Section 4.5). The circuitry is located on the Front PCB Assembly (400533), linked to the CPU by control signals and the data bus.

4.3.1 Key and LED Matrices

The keys are electrically arranged in a 8 x 7 matrix as shown in the circuit diagram. The seven columns are scanned by M5; any key contact is detected on one of the eight return lines RL_{0-7}, memorized by M6 and signal KYBDIRQ is passed to the CPU. The CPU responds by interrogating M6 Keyboard memory and acting on the specific key command.

The key LEDs are electrically arranged in an 8×4 matrix. The four rows are scanned by M4, and the eight columns receive the appropriate bit patterns from M6 display memory. This memory is up-dated as required from the CPU data bus D_0-D_7.

4.3.2 Programmable Interface M6

(Fig. 4.3.1)

M6 interfaces the keyboard and LEDs to the instrument data bus. It is addressed by $\overline{KYBDCS}$ from the digital assembly, to chip-select $\overline{CS}$ which enables commands or data to flow via the data bus DB_{0-7}. The CPU sets address A_0 to logic-Ø for data flow; but for programming the interface during initialisation or for mode change, A_0 is set to logic-1.

4.3.2.1 Read/Write Control

The $\overline{WRTSTRB}$ signal from the digital assembly is applied to M6 $\overline{WR}$. Data or Command is input to M6 from the CPU data bus during $\overline{WR}$ low and $\overline{CS}$ low, and is latched on the $\overline{WR}$ positive-going edge. The $\overline{RDSTRB}$ signal from the digital assembly is applied to M6 $\overline{RD}$. Data is output from M6 on to the data bus during $\overline{RD}$ low and $\overline{CS}$ low.

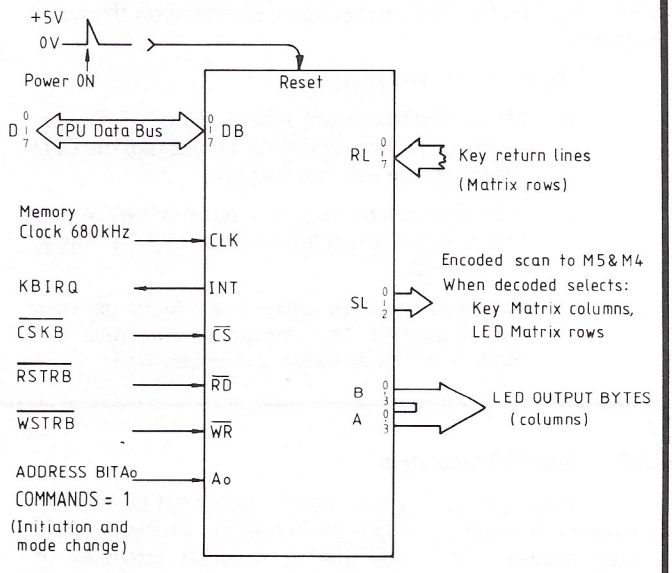


FIG. 4.3.1 M6 INTERFACE (P8279) SIMPLIFIED SCHEMATIC

4.3.2.2 M6 Initialization

When the 4200 is switched on, M6 is cleared by the PWR ON RESET pulse from the digital assembly. The interface is then programmed during initialization as follows:

Clock divider set to 'divide by eight':
The memory clock (E) at approximately 680kHz is divided by 8 to give an internal clock frequency of 85kHz.

An inherent division by 16 reduces the scan clock to 5kHz giving a scan cycling frequency of 333Hz.

Encoded Keyboard Scan:
The scan output from SL_{3-0} is a 4-bit binary count.

SL_3 is not used; SL_{2-1} scans M4, and SL_{2-0} scans M5.

Keyboard Mode:
The internal keyboard RAM is programmed as FIFO, input routed via RL_{7-0} return lines. Two-key lockout is employed with debounce.

Display Mode:
Eight character left entry for the LED display.

Inter-digit blanking: all 1's on B_{0-3} and A_{0-3} between digits.

4.3.2.3 M6 Reprogramming

The Frequency Store and Spot keys, the 12 dual ↑/↓ keys and the Zero key have a reprogrammable function. When one of these keys is pressed, the P8279 is reprogrammed into Scanned Sensor Mode. When released, the P8279 reverts to Encoded Keyboard Scan Mode.

4.3.3 Scan Decoding

The encoded scan output from M6 (approximately 333Hz cycle frequency at SL_{2-0}) is decoded by M5 to energize each key-matrix column line once every scan cycle. SL_{2-1} scan outputs are also decoded by M4 to energize each LED-matrix cathode driver once in every scan cycle for a period of two digits.

4.3.4 Key Selection

The keys are electrically grouped within a matrix of 8 rows of 7 (some positions vacant). This does not conform to their physical grouping on the front panel. The eight return lines RL_{0-7} each define a row in the matrix, whose columns are scanned by M5 (Low active).

In M6, the internally-synchronized keyboard memory stores the state of each of the 48 keys. The use of 2-key lockout rejects two or more simultaneous contacts. Any single key depression is debounced, initiating the interrupt KYBDIRQ to the CPU which then interrogates the keyboard RAM in the P8279. The next action depends upon the Key's function:

'Zero' or '↑/↓' key pressed:

a. M6 is reprogrammed into Scanned — Sensor mode for as long as the key is pressed, the CPU acting on the key information.

b. If an appropriate ↑ key is pressed while 'Zero' is held down, the resolution of the Output display is changed.

c. If a single ↑ or ↓ key is held down for longer than half a second, the display enters 'auto ↑/↓' mode, running at about 3 digits/second.

d. When the key is released, M6 is returned to Encoded Keyboard Scan mode.

'Store' or 'Spot' key pressed:

a. M6 is reprogrammed into Scanned — Sensor mode for as long as the key is pressed, the CPU acting on the key information.

b. If an F1 to F5 key is pressed while 'Store' or 'Spot' is held down, the appropriate frequency memory location is accessed, and the 4200 frequency is reset to the value in the memory.

c. When the key is released, M6 is returned to Encoded Keyboard Scan mode.

Any other key pressed (not Safety Reset):

a. M6 remains in Encoded Scan mode; the scan continues as the CPU is acting on the key information.

b. KYBDIRQ interrupts are generated only by the low-going edges of the key contact pulses, so M6 remains sensitive to subsequent key depressions.

4.3.5 Key LED Operation

After performing the change requested by the key depression, the CPU changes the bit-patterns stored in M6 internal display RAM. As this is scanned internally in synchronism with the decoded outputs of M4, each output byte of B_{0-3} A_{0-3} drives the row of LEDs accessed by M4 output lines.

The bit-pattern of the byte selects the LEDs to be lit in that row:

B_{0-3} A_{0-3} bits high = unlit,
low = lit.

During changes of output from one byte to the next, all B_{0-3} A_{0-3} lines are all set high to avoid spurious LED flashes. Transistors Q25-Q32 drive the LED anodes from a +5V supply regulated by M2, Darlington amplifiers Q21-Q24 driving the LED cathodes.

4.3.6 Audible Warning Buzzer

M48 and M1 act as a control latch for the quartz warning buzzer. With $\overline{\text{ALARM}}$ at logic-1 (+5V) M1 remains unchanged; but with $\overline{\text{ALARM}}$ at logic-Ø (0V) the state of M1 depends on the condition of Ao:

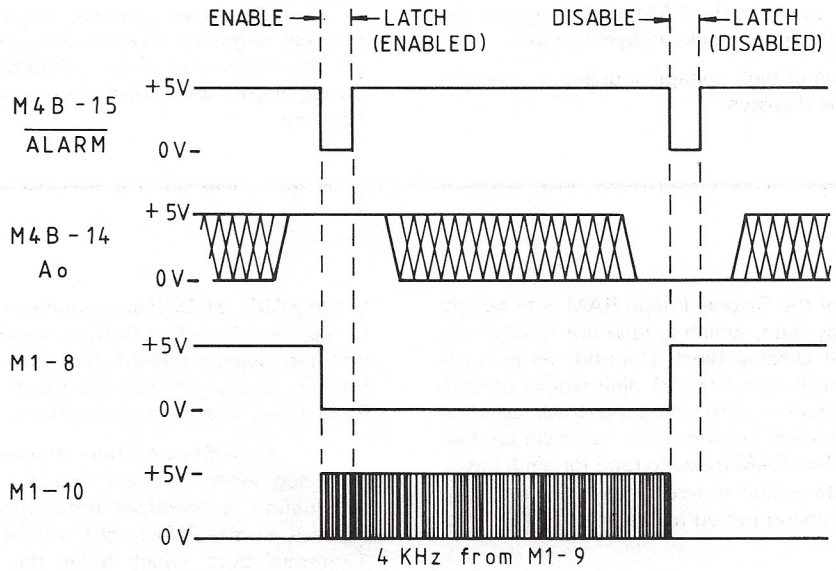
Ao at logic-1: the alarm sounds a 4kHz tone.
Ao at logic-Ø: the alarm is silent.

The latch is operated at CPU speed. Two $\overline{\text{ALARM}}$ pulses are used for each burst of sound. The first, with Ao at logic-1, starts the burst; the second, with Ao at logic-Ø, ends it. The waveforms and truth table in Fig. 4.3.2 illustrate the action of the latch.

During Power ON initialization, the combination of $\overline{\text{ALARM}}$ at logic-Ø, Ao at logic-Ø, is applied to M4B to force power-up in the disabled condition.

The 4kHz tone signal at M1-9 originates in the Precision Divider counter which is situated on the Analog Interface Assembly.
(Refer to Circuit Diagram 430570 Page 7.3-1).

Note that Ao may be used for other purposes when $\overline{\text{ALARM}}$ is at logic-1, but this will not affect the buzzer state.



M4B / M1 TRUTH TABLE

$\overline{E_B}$ ($\overline{\text{ALARM}}$)	A_B (A_o)	QO_B	$Q1_B$	M1 - 8	BUZZER
0	0	1	0	1	DISABLED
0	1	0	1	0	ENABLED
1	X	0	0	NO CHANGE	NO CHANGE

0 = 0V, 1 = +5V, X = either 1 or 0

FIG. 4.3.2 ACTION OF BUZZER CONTROL LATCH

4.4 DIGITAL DISPLAYS

The circuits described in this section perform the following functions:

(1) Storage of display data in a Display Image RAM, updated under CPU control.

(2) Generation of multiplex count which selects segment data from the RAM, and energizes the appropriate digital blocks in synchronism.

(3) Distribution of high voltage supplies to energize the plasma displays.

Part of the Digital assembly (400534) houses the display multiplexer, which includes the display image RAM, the interdigit and multiplex counters, and control circuitry.

The two plasma displays, the block multiplex decoder, segment drivers and high voltage circuits are located on the Front assembly (400533). Fig. 4.4.1 shows the arrangement and main interconnections of the display circuitry.

4.4.1 General
(Fig. 4.4.1)

The purpose of the Display Image RAM is to accept and store current display data, which is read out to drive the display segments. The Display Block Counter generates a 4-bit count at 2kHz which scans the 11 digit-blocks of both displays in parallel. The same count scans the RAM, selecting segment information for each block in turn. As there are two displays, and therefore Two RAM bytes to read for each block, the 'MODE' display data is first entered into a holding latch during the inter-digit blanking period at the start of the time-slot for its block.

To update the displayed characters, the CPU writes into the RAM at high speed (680 kHz), using signal XDDSP to connect the Address bus through the Address Source Switch to the RAM. XDDSP also connects the Data Bus to the RAM through the Data Bus Buffers, writing the new segment data into the selected RAM Address. The high speed of the transfer, compared with the much slower scanning speed in Read mode, avoids spurious effects appearing on the displays.

Each RAM address contains only 8 bits, but there are nine segments in each display block. Comma-segment information is therefore not written into its normal block address in the RAM, but stored as a bit in a separate 'Commas' byte, which holds the data for all eight blocks which have a comma. The byte is read out into a Commas Data Holding Latch, once every block-scan cycle, and then selected for display by a Commas Multiplexer 8-into-1 switch.

4.4.2 Static Conditions
(Circuit Diagram 430533 Page 7.1-2)

The plasma displays are driven from +5V (anode supply) and -175V (cathode supply). The supplies are connected by conduction of anode and cathode driver transistors:

Anodes:
Both Displays — Q10 to Q20,

Cathodes:
MODE Display — Q2 to Q9, and Q41,
OUTPUT Display — Q33 to Q40, and Q42.

When not energized, all anodes and cathodes are held at −70V by the action of 75V zener D17.

To energize a particular block, (on both displays simultaneously), the multiplex decoder causes the relevant anode driver transistor to conduct, and lift its two anodes to +5V.

At the same time the two sets of data, for the characters to be displayed in the two blocks, are extracted from the Display Image RAM and applied to the segment cathode drivers. Those segments selected for illumination are pulled to −175V, striking the discharge.

Four keep-alive electrodes in each digit block, two anodes and two cathodes, are maintained at voltages of +5V and −175V respectively. This ensures a rapid strike when a digit is energized, and helps to prevent inter-block 'streaming'.

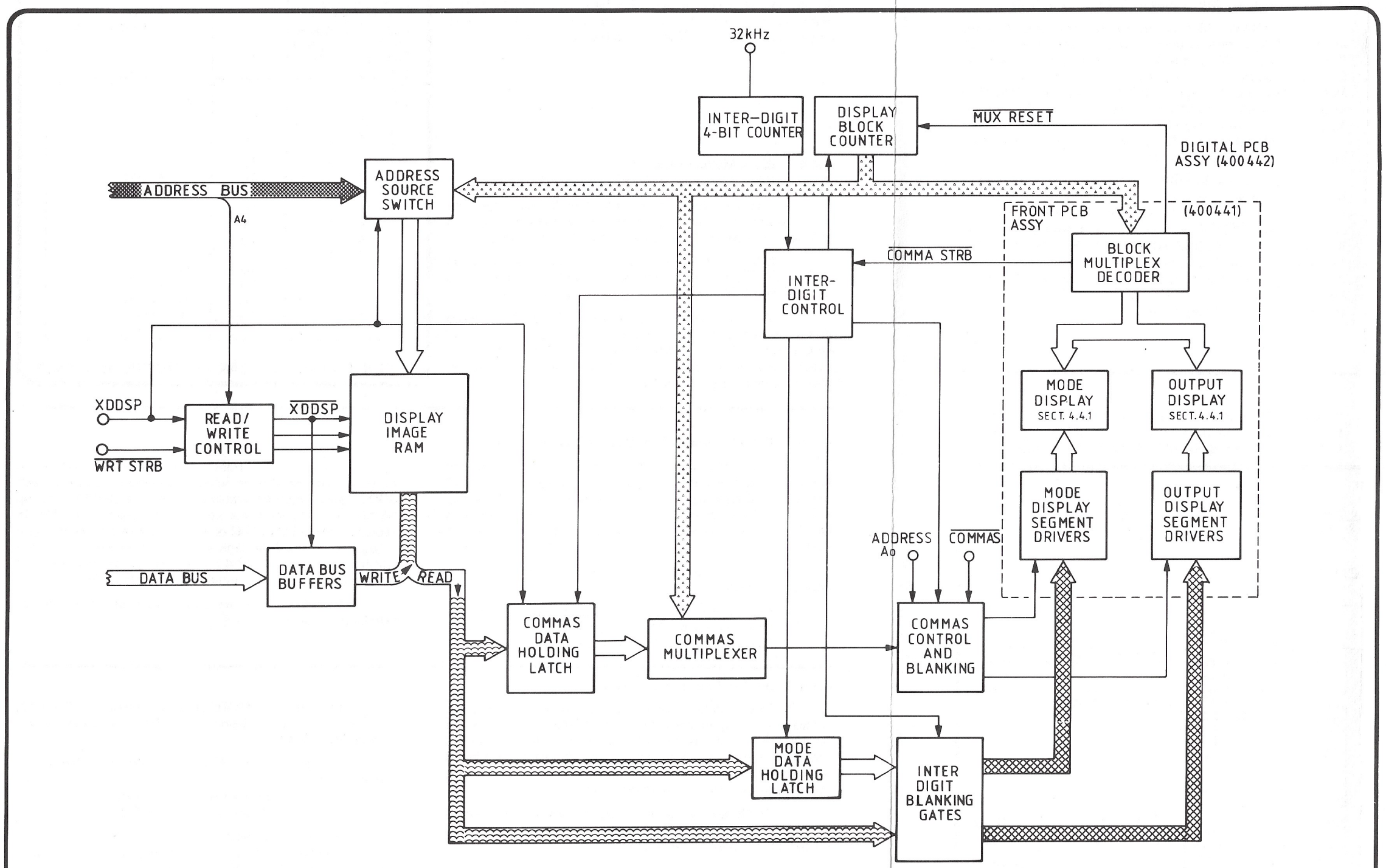


FIG. 4.4.1 MODE AND OUTPUT DISPLAYS—FUNCTIONAL BLOCK DIAGRAM

4.4.3 Write Mode
(Fig. 4.4.2)

Whenever the CPU is programmed to update a display (e.g. Range, Function, Mode or Value change) it sets address decode XDDSP to logic-1 with each byte of data to be transferred. This causes M31 and M33 to select the CPU address lines A_{4-0} which are mapped directly to the RAM address input lines A_{4-0}. The RAM is placed into its write mode by signal XDDSP at logic-Ø (M17-8, TP5, M16-16).

The RAM M16 is divided into two sections, using the address bit A_4 to differentiate between OUTPUT and MODE Display images. When the CPU is loading the RAM with OUTPUT Display data, it sets A_4 to logic-1, translating to set M16-19 (A4) input to logic-1. MODE Display and COMMAS images are written into M16 with A4 at Logic-Ø (M33-4 and 13 at Logic-1 in write mode).

(In Read mode M16-19 is again used to differentiate between the two image sections).

The signal $\overline{\text{XDDSP}}$ (M17-8) enables the tri-state buffers M1 and M2, connecting the CPU data bus to M16 data input/output lines D_{0-7}. The CPU also generates the write strobe signal $\overline{\text{WRTSTRB}}$ with each byte of display data. This is combined with XDDSP (M17-6, M16-10, TP4) to enable M16 internal Input/Output tri-state buffers to accept the data byte (chip select CS_0). Once the display data has been loaded into the RAM, the CPU returns XDDSP to logic-Ø and the RAM reverts to Read mode.

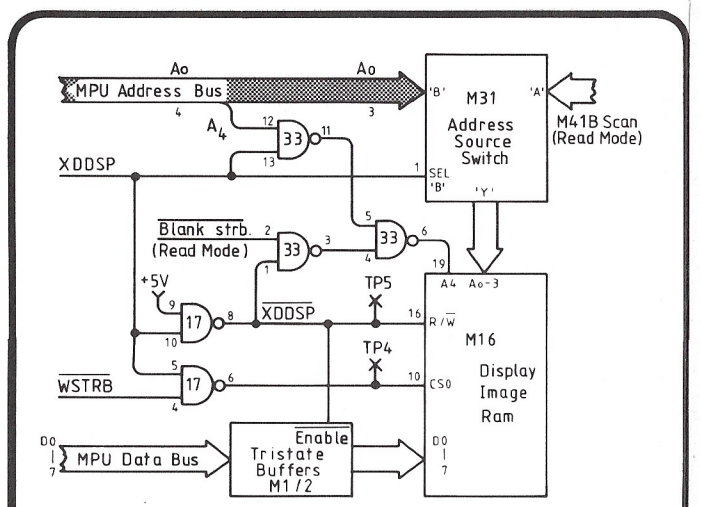


FIG. 4.4.2 RAM ACCESS—WRITE MODE LOGIC

4.4.4 Read Mode
(Fig. 4.4.3)

Unless the CPU has data to update, the signal XDDSP remains at logic-Ø, to hold the display multiplexer circuitry in Read mode. The RAM data bus is isolated from the CPU data bus by tri-state buffers M1/M2, and M16 is chip-selected in read mode by M17-6 and M17-8 at logic-1.

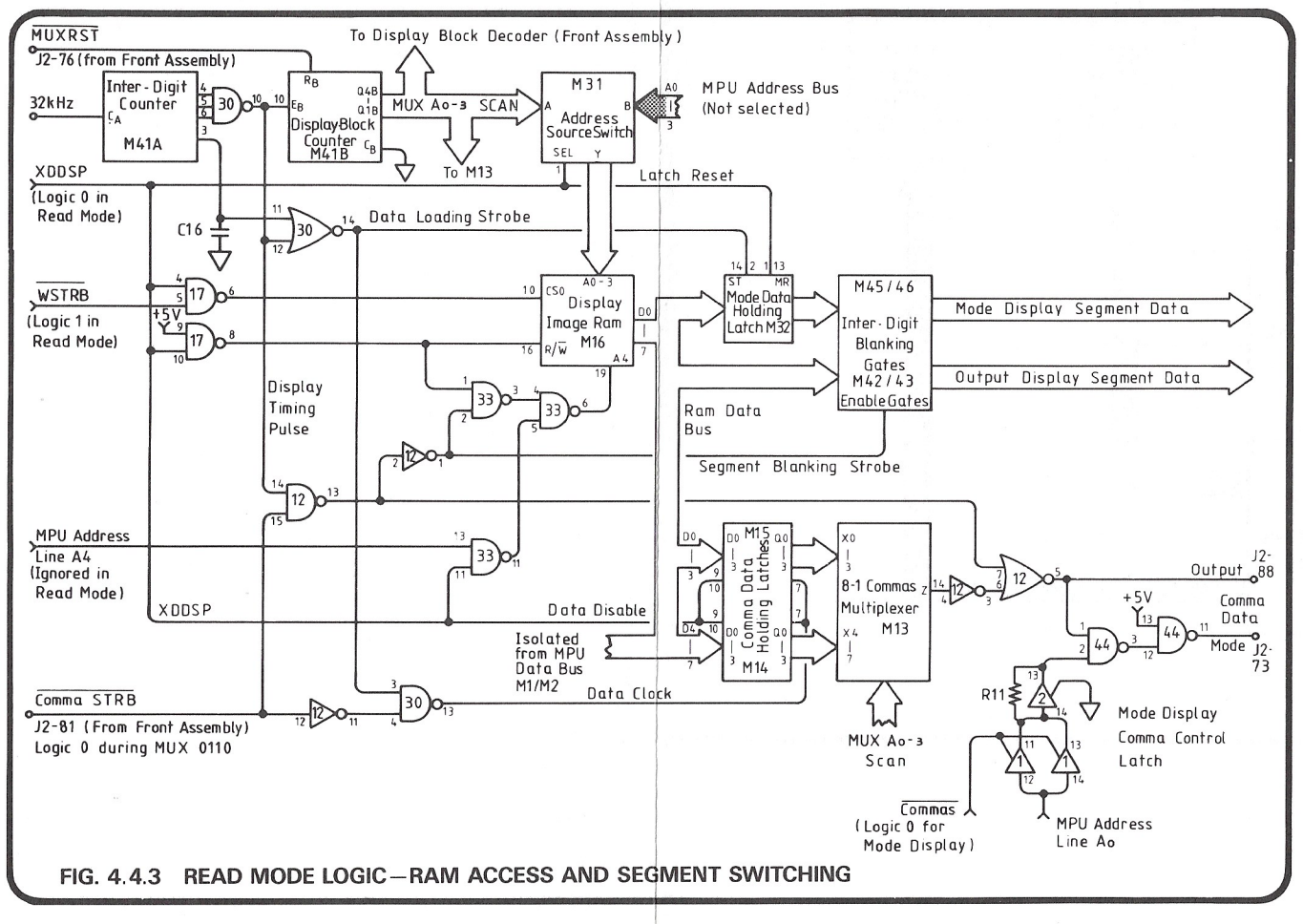


FIG. 4.4.3 READ MODE LOGIC—RAM ACCESS AND SEGMENT SWITCHING

4.4.4.1 Display Scan Address Interlacing
(Figs. 4.4.3 and 4.4.4)

M31-1 (SEL) at logic-Ø causes the RAM to be addressed from the display block scan, mapping M41B outputs: Q4B, Q3B, Q2B, Q1B to RAM address input lines: A_0, A_3, A_2, A_1 respectively. This bit-rotation interlaces the extraction of display data, in synchronism with the interlaced block selection by the Front Assembly Scan decoder.

4.4.4.2 Block Multiplex Decoding
(Circuit Diagram 430533 page 7.1-2)

The 4-bit Block scan output MUX A_{3-0} from the multiplex scan counter M41B (dig) is used at $DATA_{4-1}$ input to M3, which decodes it into a low-active 16-line scan S_{15-0}.

M3 output S_6 generates the comma strobe signal $\overline{\text{COMMA STRB}}$, S_{13} terminates each scan by resetting M41B (dig) ($\overline{\text{MUX RESET}}$), and S_7, S_{14} and S_{15} are not used.

The other eleven outputs from M3 switch Q10-Q20 on sequentially, to drive the anodes of both plasma displays in synchronism. As can be seen from Fig. 4.4.4, the interlace is maintained to avoid consecutive activation of adjacent blocks, thus preventing inter-block 'streaming'.

MUX A_{3-0} SCAN				M3 (Front Assy.)	
A_3	A_2	A_1	A_0	M3 Output (Low Active)	Energised Line (Both displays' Anodes and Signals)
M_3 $DATA_{4-1}$ Input					
D_4	D_3	D_2	D_1		
M_{16} (Dig Assy.) A_{3-0} Input (Display Image RAM)					
A_0	A_3	A_2	A_1		
0	0	0	0	S_0	A_1
0	0	0	1	S_1	A_3
0	0	1	0	S_2	A_5
0	0	1	1	S_3	A7
0	1	0	0	S_4	A_9
0	1	0	1	S_5	A_{11}
0	1	1	0	S_6	$\overline{\text{COMMA STRB}}$
0	1	1	1	S_7	Not used
1	0	0	0	S_8	A_2
1	0	0	1	S_9	A_4
1	0	1	0	S_{10}	A_6
1	0	1	1	S_{11}	A_8
1	1	0	0	S_{12}	A_{10}
1	1	0	1	S_{13}	$\overline{\text{MUX RESET}}$
1	1	1	0	S_{14}	Not included in cycle ($\overline{\text{MUX RESET}}$ at S_{13})
1	1	1	1	S_{15}	

FIG. 4.4.4 DISPLAY SCAN ENERGISING SEQUENCE

4.4.4.3 OUTPUT And MODE Display Data Selection

When the processor writes display data into the Display Image RAM, the A_4 input is used to select the MODE or OUTPUT Display data storage area (see para 4.4.3 and Fig. 4.4.4). In Read mode also, A_4 is set to logic-1 to read OUTPUT Display data, and to logic-Ø for MODE or COMMA data.

For an alpha-numeric display block, 18 bits of data could be required:

One byte for the OUTPUT Display block segments;
One byte for the MODE Display block segments;
Two bits for COMMAS (one for each display).

The problem of transferring two bytes of data along the single-byte RAM data bus is overcome by strobing each MODE display segment byte into a holding latch (M32), during the first 30μs of its block selection time-slot. The MODE display section of the RAM is selected by setting its A_4 input to Logic-Ø for this 'Inter-digit' period, during which the inter-digit blanking gates (M42/43, M45/46) set all segment lines to the Front Assembly to logic-Ø (segments OFF).

COMMAS data are stored as a separate byte as described in Section 4.4.4.6.

4.4.4.4 Display Timing (Fig. 4.4.5)

Read mode is driven by a 32kHz square wave (Waveform 'A', generated from the 13-bit counter in the Analog Interface Assembly M15-11), used as clock for a 4-bit counter (M41A). The three most significant bits are combined at M30-10 to produce Waveform B, the display master-timing pulse, used also for Inter-digit blanking.

The following example explains how the display data is set up for the next display block in sequence, during the 62.5μs of the display timing pulse.

EXAMPLE

Initial State:
M41B count has already reached 1001, and the block 4 anodes of both displays are energized (Fig. 4.4.4).

The OUTPUT Display data for block 4 is selected in the Display Image RAM (M16) to drive the segment cathodes for a figure '6', which appears on the OUTPUT Display.

Block 4 of the MODE Display is showing a figure '3', and the data for this is being output from the Mode display holding latch (M32).

The data held in M16 for the next byte (Block 6 of both displays) is:

OUTPUT Display — Figure '8'
MODE Display — Figure '7'

Block Changeover:
The next block is selected during the display master timing pulse (Fig. 4.4.5, Waveform B).

a. The negative-going leading edge triggers the scan counter (M41B) whose output advances to 1010 (block 6). On the Front Assembly, M3 de-energizes A_4 anodes and energizes A_6 anodes.

b. For the duration of the display master timing pulse (Logic-Ø at M12-14), the A_4 input to M16 is set to Logic-Ø as A_{3-0} inputs are advanced to 0101. Mode display data for figure '7' is loaded onto the RAM data bus as follows:

i) M17-6 at Logic-1 chip-selects M16 at M16-10,

ii) M17-8 at logic-1 holds M16 in Read mode,

iii) RAM address A_{4-0} = 00101 reads block 6 MODE Display data onto the RAM data bus (M1/M2 isolates from the CPU data bus),

iv) M30-14 at logic-1 strobes the byte into M32 during the 30μs of Waveform D, then returns to logic-Ø leaving figure '7' data latched at M32 output.

v) M12-1 at logic-Ø blanks the two displays by setting M45/M46/M42/M43 outputs to logic-Ø, regardless of their inputs from M32 and the RAM data bus.

c. The positive-going edge of Waveform 8 lifts the RAM A_4 input (M16-19) to logic-1, addressing the OUTPUT Display section of memory. A_{3-0} is still at 0101, selecting block 6 display data (in our example a figure '8') which it loads on to the RAM data bus.

The end of the master timing pulse also releases the blanking by enabling the gates M42/M43/M45/M46, so the data for both MODE and OUTPUT Displays are now delivered to the cathode drivers on the Front Assembly, to strike the gas discharge in the two energized A_6 blocks.

This condition persists for 437.5μs until the next master timing pulse, when Waveforms B and C repeat the process for the next block of stored display data.

At any time during the cycle, the CPU may force Write mode. This will not disturb the scan from M41B, but XDDSP will reset M32 outputs to logic-Ø (M32-1/13). However, the speed of byte transfer from the CPU ensures that transferring data is not visible on the displays. Subsequently, each block will be driven by its new stored data.

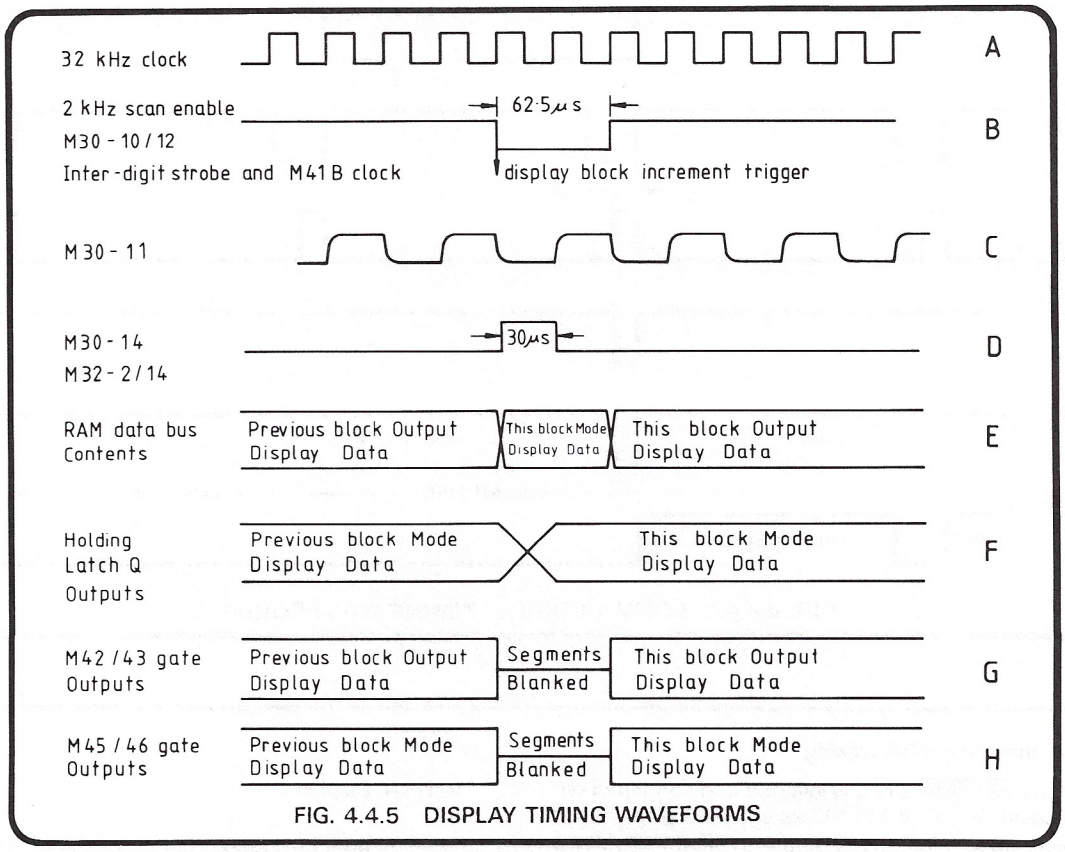


FIG. 4.4.5 DISPLAY TIMING WAVEFORMS

4.4.4.5 Display Segment Drive

(Circuit Diagram 430533 Page 7.1-2)

The strobed segment signals from the Digital Assembly are input to the Front Assembly on J1-67 to J1-75 (MODE Display) and J1-82 to J1-90 (OUTPUT Display). These are already synchronized to their blocks by the 4-bit block scan MUX A_{3-0} within the Digital assembly.

For each block in sequence, the appropriate segment bit-pattern is set at the input to the segment drivers. For bits at logic-1, the rise is passed through line capacitors to reverse-bias DC restoration diodes and forward bias their driver - transistor bases. The resultant collector currents pull the segment cathodes from their quiescent −70V, to −170V. The correct block anode is simultaneously lifted from −70V to +5V by its anode driver transistors, striking the gas discharge and displaying its digit. For bits at logic-Ø the cathode drivers remain cut off.

The driver emitter resistors control the segment cathode currents for uniform brilliance.

During change-over between blocks, all segment inputs at logic-1 are returned to logic-Ø by the inter-digit blanking strobes M42/43/45/46 (dig). This turns off the drive transistors and blanks the display. The high scan frequency and persistence of the operator's vision prevent the blanking being observed on the display.

4.4.4.6 Comma Logic

(Fig. 4.4.6)
(Circuit Diagram 430534 Page 7.2-1)

The comma is the ninth segment (i) in each of the numerical display blocks. It cannot fit into a block's byte in memory, as there are only eight bits per byte. But all the comma information can be stored in a single byte of memory in the RAM (RAM address 01100). This is possible although there are nine numerical blocks, because the ninth block never requires a comma. Legend blocks A_{10} and A_{11} do not have a segment (i).

The RAM COMMA data is updated by the CPU in Write mode, and is read out (as though it were another display block) by M41B scan 0110 during the master display pulse (Waveform B sets RAM A_4 input to logic-Ø). The same MUX combination 0110 selects S_6 output from M3 decoder on the Front Assembly, which sets the signal $\overline{\text{COMMA STRB}}$ to logic-Ø.

Thus for the duration of $S_{6=0}$ (500μs), the COMMA data is on the RAM data bus, but the blanking gates prevent it reaching segments (a)-(h).

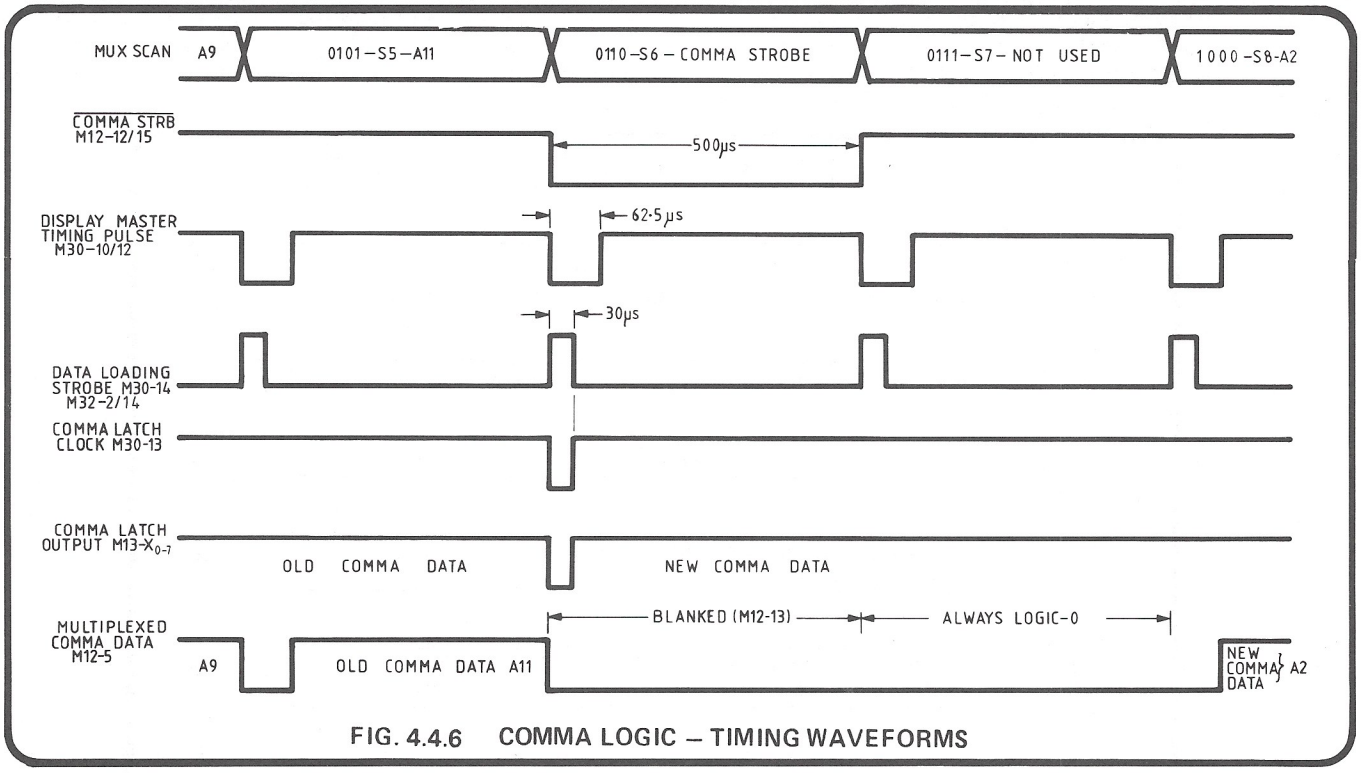


FIG. 4.4.6 COMMA LOGIC – TIMING WAVEFORMS

4.4.4.7 Comma Drive Multiplexing

Signal $\overline{\text{COMMA STRB}}$ is inverted and combined with the Data Loading Strobe at M30-13 as a logic-0 pulse, whose positive-going edge clocks the comma data into latches M14/15, approximately 30μsec after it has been loaded on to the RAM data bus. The permanently-enabled outputs from these latches are input as X_{0-7} into the 8-into-1 multiplexer M13 for a complete MUX scan until the next $\overline{\text{COMMA STRB}}$ signal.

The block-multiplex scan from M41B selects the correct X input to synchronize with activation of its display block anode. This is output from M13-14(Z), into blanking gates M12.

Comma information is blanked during $\overline{\text{COMMA STRB}}$ and by inter-digit blanking during display-block change-over (M12-7).

The Comma drive line from M12-5 to the front panel via J2-88, controls segment (i) cathode driver for the OUTPUT Display.

If commas are required on the MODE Display (e.g. in 'Spec' operating mode +Lim or −Lim) they will always be in the same display blocks as the OUTPUT Display. When this mode is selected, the CPU pulses the $\overline{\text{COMMAS}}$ line to logic-Ø at the same time as Address line A_0 goes to logic-1. Tristate buffer outputs M1-11 and 13 go to +5V, setting M2-13 output to +5V (logic-1). Outputs M1-13 and M1-11 go tristate when the $\overline{\text{COMMAS}}$ line returns to logic-1, leaving M2-13 latched to +5V by the positive feedback action of R11. So M44-2 enables the comma data to the MODE Display segment driver via J2-73 to copy the OUTPUT Display commas on to the MODE Display.

When Mode display commas are not required, A_0 is set to logic-Ø (0V) with $\overline{\text{COMMAS}}$ signal at logic-Ø. Thus M2-13 latches to logic-Ø and M44-2 disables the flow of comma data to the Mode display.